Synopsis V1.0
Single Event Transient and Destructive Single Event Effects Testing of the Linfinity SG1525A Pulse Width Modulator Controller

Jim Howard[1], Marty Carts[2], Jim Forney[1], and Tim Irwin[3]
1. Jackson and Tull Chartered Engineers, Washington DC 20018
2. Raytheon ITSS, Greenbelt, MD 20771
3. QSS, Inc., Greenbelt, MD 20771

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I. Introduction

This study was undertaken to determine the single event destructive and transient susceptibility of the Linfinity SG1525A Pulse Width Modulator Controller. The device was monitored for transient interruptions in the output signals and for destructive events induced by exposing it to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility.

II. Devices Tested

The SG1525A Pulse Width Modulator controller integrated circuit contains all logic and drivers required to implement all types of switching power supplies. It contains a 1% voltage reference, an oscillator with synchronization capability (to synchronize multiple devices), a pair of power Field Effect Transistor (FET) drivers, programmable dead time control (to ensure one FET is off before the other begins to turn on), soft start circuitry, shutdown control, under-voltage shutdown, and a pulse latch-off circuit (to prevent any pulse, once terminated, from turning on again). The drivers sink and source 200 mA, and are normally low (other variants offer normally high outputs). The oscillator runs from 100 to 500 KHz. The device operates from 8 to 35 V_{dc} input, and the DUT logic and the output drivers have independent supplies (V_{in} and V_c, respectively). It is available to 883B Standards. Appendix A is the manufacturer's datasheet.

The device under test (DUT) is packaged in a 16 pin ceramic DIP, manufacturer's package type J. This type of package construction is analogous to Oreo™ construction, where the two outer ceramic (chocolate) layers sandwich a cement-like (beef fat/sugar/titanium dioxide) layer. Within a cavity in the center of the middle layer the die is mounted and is wire-bonded to the lead frame. The leads exit the package thru the lower portion of the middle layer. The DUTs tested with heavy ions were de-lidded to allow the limited range ions access to the active layer of the die. The cleave point was just below the upper chocolate layer of the package, leaving the lower and middle layers with leads intact. Five DUTs were de-lidded with 100% success rate.

All DUTs' package markings were identical and are given in the table below:

TOP	BOTTOM
SG1525AJ/883	113088T EA
34333 PHIL	PHILLIPINES
_1A0126PQ	

The sample size used during the testing was four devices. The devices were manufactured by Linfinity and were characterized prior to exposure. The devices tested had a Lot Date Code of 0126.

III. Test Facility

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 15 MeV/amu tune.

Flux: 1.4×10^4 to 4.4×10^4 particles/cm^2/s.

Ion	Incident LET ($MeVcm^2/mg$)
Ar	8.6
Kr	28.7
Xe	53.1

IV. Test Methods

The application for which these tests were conducted has two DUTs, termed the Master and Slave devices. They are synchronized together via the SYNC line out of the Master device and the Master device driven by an external 200 kHz reference frequency source (Normal mode). In the absence of the external frequency reference, the application circuit was designed to self-oscillate at some lower frequency, thus not losing total functionality (Free-run mode). The source voltage for both the DUT logic and the output driver collectors was 10.75 V_{dc}. Each DUT in the application circuit drives a pair of FETs, each at half the oscillator frequency, and each out of phase with the other. The FETs drive either end of a center-tap grounded transformer primary to ground when driven high (turned ON) by the DUT. The output of each DUT's transformer had multiple outputs, which were rectified and filtered.

The DUT is designed for voltage feedback in order to modulate the width of each output pulse to maintain final filtered voltage stability. However, this application drives the outputs at maximum (50% duty cycle minus dead time of approximately 5%) with no feedback.

Figure 1 shows the functional block diagram of the SG1525A. The output of the DUT is a pair of pulse trains for driving FETs, which drive a transformer, whose output(s) are then rectified and filtered. Reproducing the totality of this circuit, especially the FETs and transformer, was deemed cumbersome and of little value. Instead of trying to determine SEE from the filtered DC of the circuit's output, the DUT outputs were monitored, with simulated FET loading, for deviation from the nominal waveforms. Knowledge of the dynamics of the application circuit will allow the application circuit designers to determine the end effects of any observed single events on the output voltages.

The application circuit's topology was reproduced for the DUTs, with some limitations and modifications. The input voltage source was driven by an HP6626A power supply instead of a switching supply and the reference frequency input was supplied by a pulse generator. Also, the gates of the radiation-hardened power FETs (and all

following circuitry, transformers, rectifiers, filter capacitors, were simulated by an equivalent capacitance. The application FETs, IR IRHF57130 100V N channel enhancement mode radiation hardened FETs, have a C_{iss} (gate-source capacitance) of 1038 pF typical and C_{rss} (gate-drain capacitance) of 45 pf. The Miller effect can magnify the effect of C_{rss}, but at a V_{ds} of only 10.75 V this did not have a significant effect in this case. The FET was simulated with a mica, 1100 pF capacitance to ground. The application circuit's 100 Ω series gate resistors were, of course, included in the test circuit.

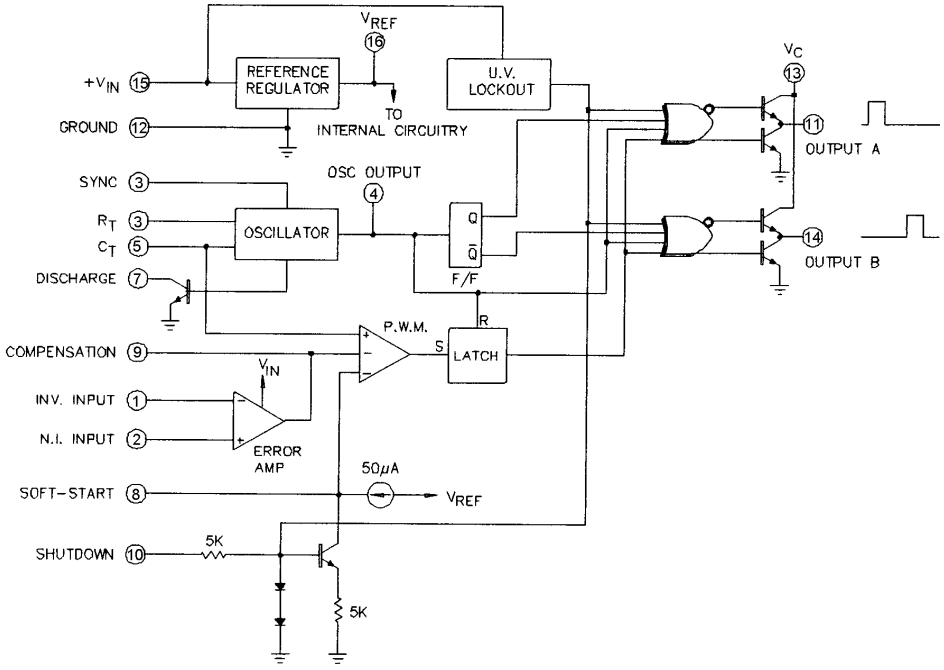


Figure 1. Functional Block diagram of the SG1525A.

Two iterations of the two DUT circuit were built on a protoboard using good RF practices (specifically, ground plane and layout which minimized high frequency and power supply bypass capacitor trace lengths). Power and frequency reference were switched between circuits by relays. DUT outputs were not switched in order to maintain signal edge fidelity. Rather, all eight (two per DUT) probe coaxial cables were brought out to an area of the facility which is accessible by interlock suspension, so that switching operation from one DUT to another could be affected fairly rapidly. Relays were actuated by otherwise unused power supply outputs. Each DUT within a circuit was supplied by a separate supply so that individual DUT currents could be monitored (See Figure 2).

The DUT outputs were monitored directly at the DUT IC pins. Normally, low capacitance FET probes would be used to monitor signals with low loading effect, but in this case the 8 V linear range of the probes was too low to monitor the almost 11 V_{pp} signals. Instead, a high impedance high bandwidth probing technique was employed. A 5 kΩ resistor and a 50 Ω resistor (involving a length of 50 Ω coax plus the scope's 50 Ω termination resistance on the far end) formed a resistive divider (giving input signals at

the scope reduced by approximately a factor of 100). The 5.05 kΩ load on the DUT pin was negligible. The bandwidth of the circuit is shown to be quite sufficient for these purposes. The 15-foot long coaxial cable and the oscilloscope's termination resistance is integral to the probe's operation, but BNC connections were put on board for ease of use. Appendix B shows material from reference [3] and calculations supporting this technique. Appendix C is the application FET datasheet. Also note that the output B signal was offset in voltage at the scope by approximately 10 mV, allowing for better monitoring of both output channels.

The triggering mode used to capture radiation-induced events was set to the pulse mode. In this mode, the scope will trigger when it sees an input pulse that is smaller than a given amount of time. This method was chosen since the expected error types would either be the shortening of one output pulse or the loss of a sequence of output pulses. Therefore, if a positive pulse was not observed within a given time, lasted for less than a given time, or the off time was smaller than the given time, the scope would trigger (capturing the expected error types). Unfortunately, an unanticipated error type was also observed where the outputs of the two channels were high simultaneously (the widths of the pulses may or may not be shortened). Unless there was another event occurring, the scope would not trigger on these overlap events. Therefore, as will be discussed later in detail, the measured event rates for these overlap events is smaller than actual due to the triggering mechanism not being specifically set to capture these types of events.

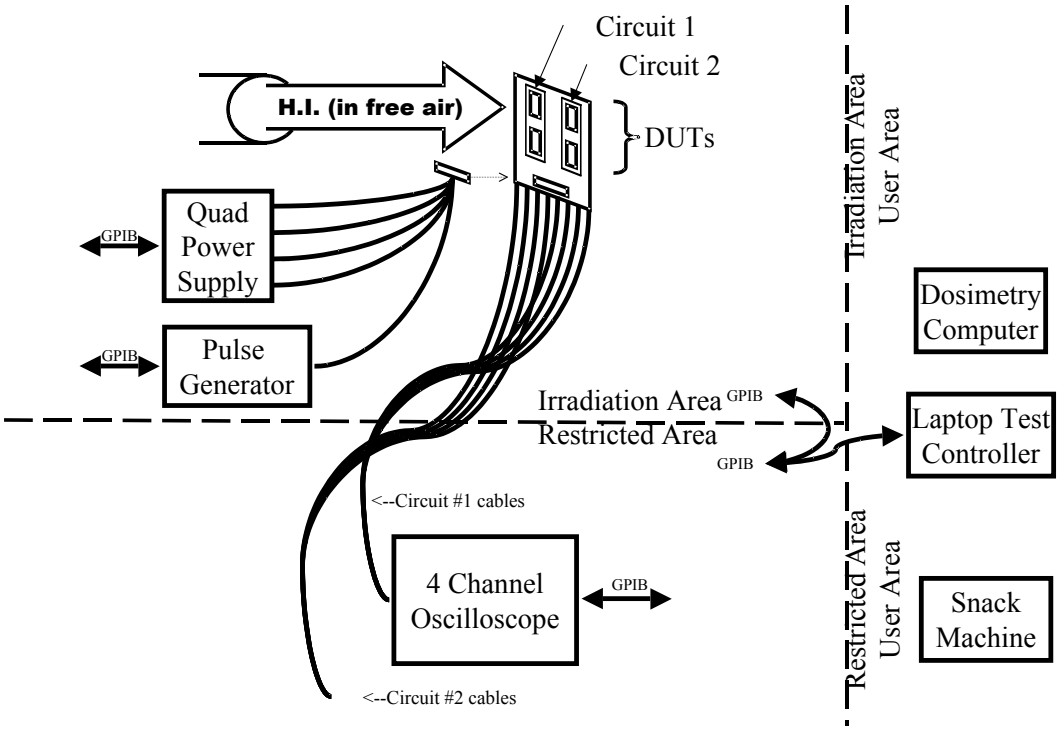


Figure 2. Block diagram of the test setup.

The test flow for these devices included testing of both modes of operation (Normal and Free-run) and exposing both the Master and Slave devices to the ion beam. For these four test conditions, the output of either the Master or Slave device is monitored at the

oscilloscope, leading to eight test conditions at each effective LET. DUT angles of either 0, 30, 45, or 60 degrees were used to achieve an effective LET range from 8.6 to 61.3 MeV-cm^2/mg. This process was completed for two sets of devices, yielding the sample size of four. Finally, on one DUT at the higher normal incidence LET of 53.1, the V_{ds} was raised to 12 volts to perform a worst-case latchup test.

V. Results

Single Event Latchup

Four parts, biased at nominal voltage (10.75 volts), were tested with heavy ions with LETs ranging from 8.6 to 61.3 MeV-cm^2/mg. Additionally, one part was exposed to an ion beam with an LET of 53.1 while biased at 12 volts. These conditions were run while the devices were operated in both the Normal and Free-run modes. In no test condition were any high current conditions observed that would indicate any latchup or other destructive mode. Therefore, the SG1525A is considered to have an LET threshold for destructive events of greater than 61.3 MeV-cm^2/mg.

Single Event Transients/Upsets

Normal outputs from the SG1525A are shown in Figure 3 for the two modes of operation (recall that the signal levels are 100X reduced and the channel B signal is offset for easier viewing). When exposed to the heavy ion irradiation, three primary modes of altering this output were observed. These were termed simple, double and overlap. A simple event is one in which the only observable difference is that one output pulse is either shortened or missing.

A double event is one where the output of one of the channels goes high consecutively, rather than alternate with the opposite channel. It should be noted that the majority of the double events were seen on channel B output. However, that is simply due to the triggering scheme used. There is no indication in the data sheet that would indicate either channel having a preference for these double events.

The overlap event is one in which the two channels lose their sync and the output "highs" and "lows" overlap. This overlap condition can exist for very short periods of time to complete overlap. The distribution of percent overlap appears to be uniform in time, indicating no preference or mode for initiating this overlap condition. Finally, it should be stated that the observed overlap events do not necessarily give a complete picture of the events and their true rate. This is due to the triggering scheme used for this testing. Some events that were captured saw the initiation of the overlap condition. However, other events were captured that showed the overlap condition existing prior to the trigger point, indicating that the overlap condition was initiated some time earlier but was not seen until a proper trigger event occurred. However, it is not believed that this loss of sync is a long-term event, as the overlap condition (whether overlapped or not or the percent overlap) did not persist from one trigger event to the next (typical event rates were less than one per second). To get a more accurate indication of the overlap event onset and event rate, more testing with logic triggering (trigger when both outputs go "high") will be required.

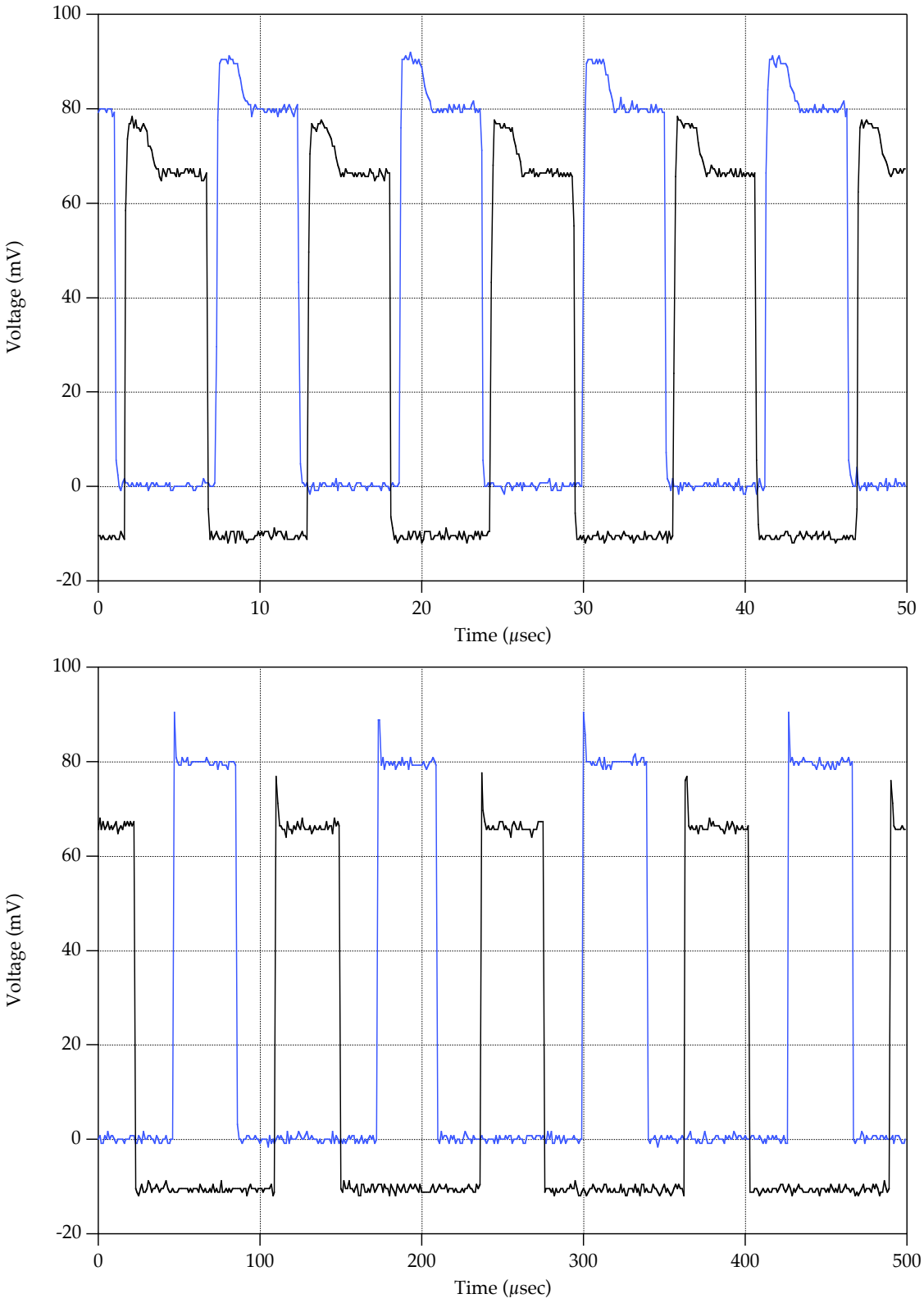


Figure 3. Pre-rad traces for Normal (top) and Free-run (bottom) modes.

Finally, at high LETs, some events occurred that could not be categorized into one of these three modes. These are considered "other" events but are not considered significant, as they didn't occur until very high LETs. Samples are included in this report to indicate the other types of events that could be possible.

Sample output for each of the modes of upset and the modes of operation are given in Figure 4 through Figure 19. Figure 4 through Figure 8 show the simple, double, overlap and other events for LETs of 8.6, 28.7 and 53.1 MeV-cm^2/mg for the Normal mode of operation and irradiating and observing the Master device. Figure 9 through Figure 11 show the simple, double, overlap and other events for LETs of 8.6, 28.7 and 53.1 MeV-cm^2/mg for the Free-run mode of operation and irradiating and observing the Master device. Figure 12 through Figure 15 show the simple, double, overlap and other events for LETs of 8.6, 28.7 and 53.1 MeV-cm^2/mg for the Normal mode of operation and irradiating and observing the Slave device. Figure 16 through Figure 19 show the simple, double, overlap and other events for LETs of 8.6, 28.7 and 53.1 MeV-cm^2/mg for the Free-run mode of operation and irradiating and observing the Slave device.

The second issue to deal with in transient/upset characteristics is the cross section. Figure 20 and Figure 21 show the cross section versus effective LET curves for the Normal and Free-run modes of operation while irradiating and monitoring the Master device. Figure 22 and Figure 23 show the same curves while irradiating and monitoring the Slave device. For all these figures, the cross section for all events (Total), double events, and overlap events is plotted. Weibul fits to these data sets are also plotted, as appropriate.

The first comment is that the Weibul fit to the Total cross section appears to be independent of mode of operation and device struck (as the Weibul curve plotted is the same for all four figures). This curve shows an onset threshold LET of approximately 5 MeV-cm^2/mg and a saturation cross section of approximately 1 x 10^{-4} cm^2. The curves for the double and overlap events may show some dependence on the mode of operation and device irradiated. They do show a smaller overall saturation cross section and possibly higher threshold LETs. However, to fully evaluate these statements, additional testing with triggering modes to fully capture all double and overlap events is needed as well as testing at LETs less than 8.6. Additionally, as the LET threshold is low, proton testing would also need to be done to fully evaluate these devices for space operations.

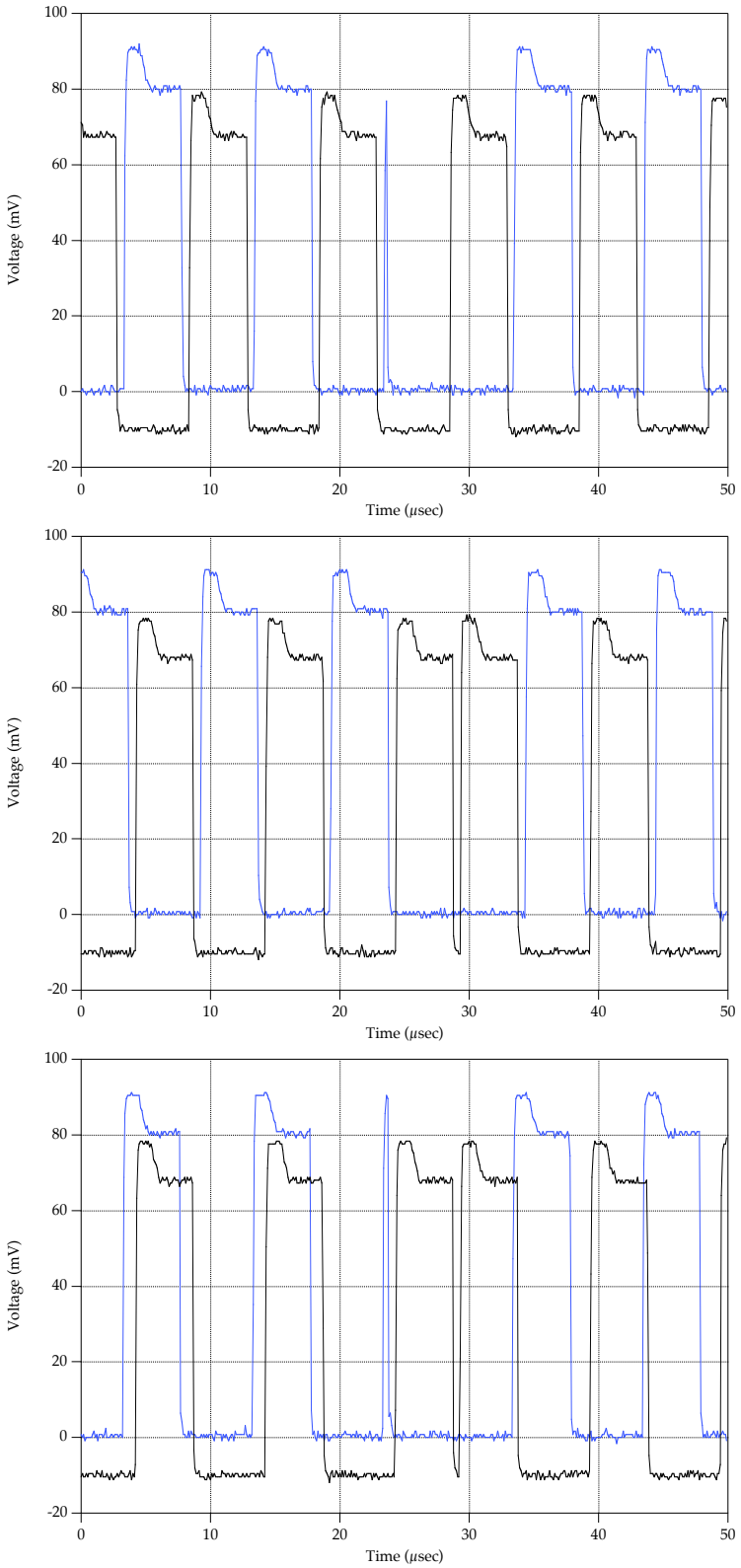


Figure 4. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Normal mode and the LET was 8.6.

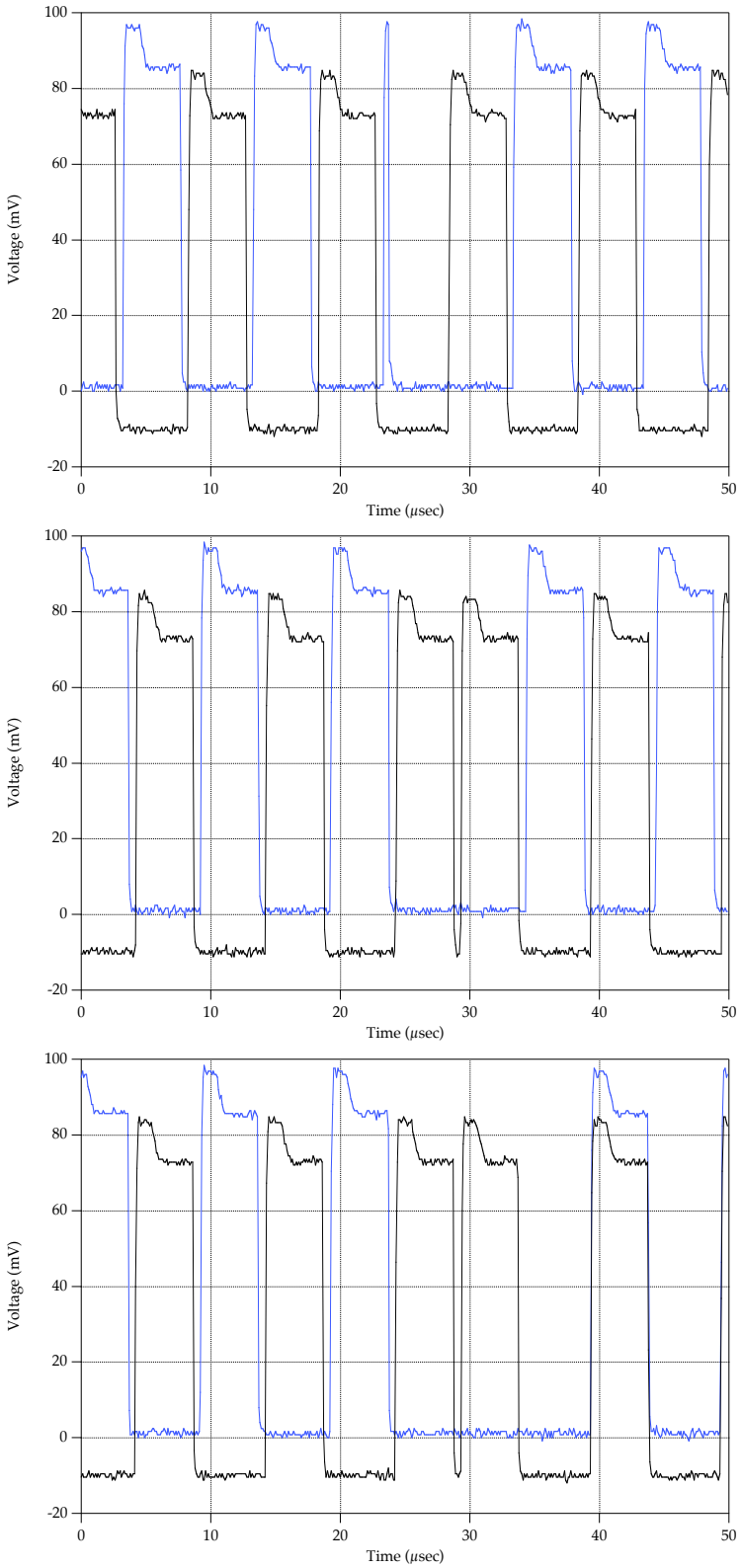


Figure 5. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Normal mode and the LET was 28.7.

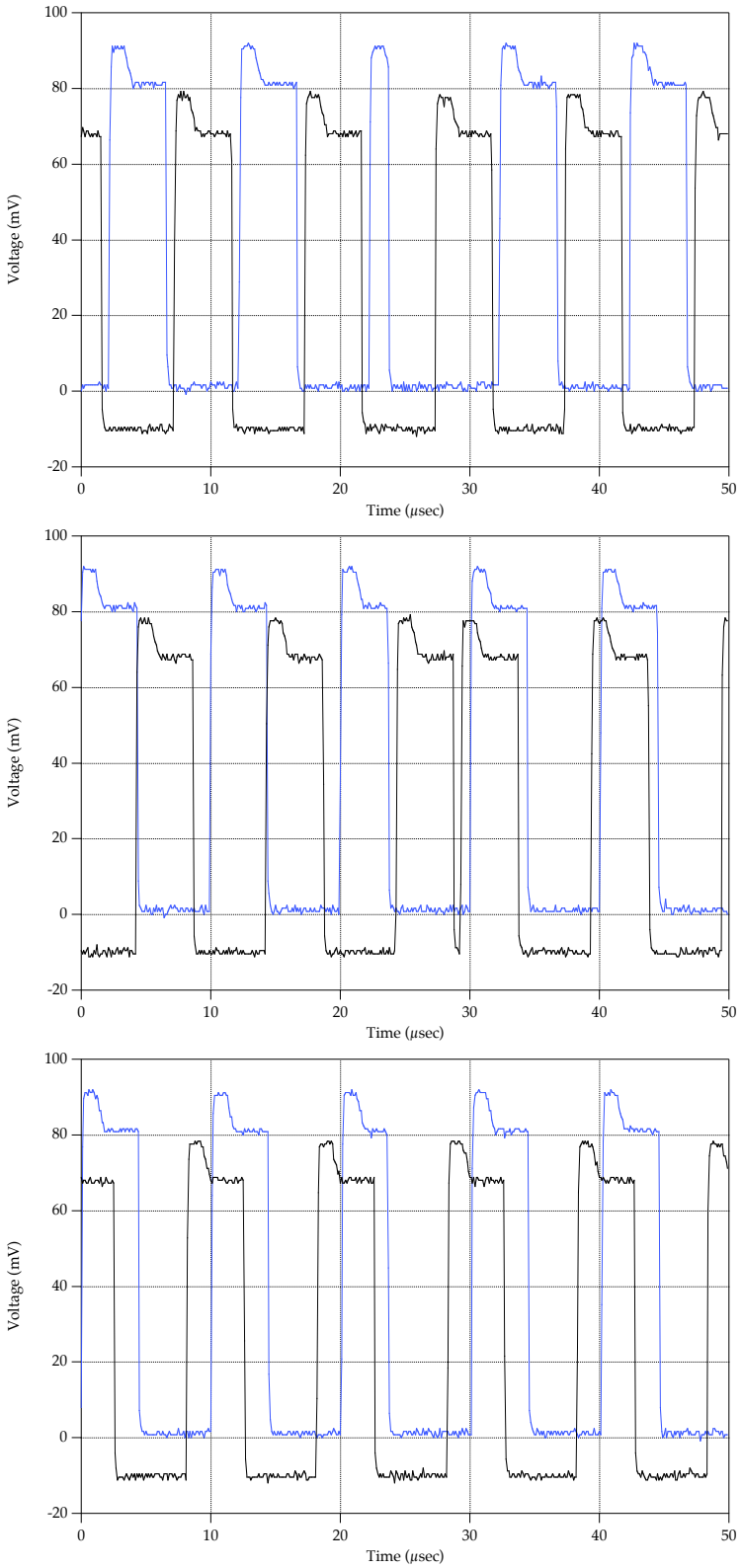


Figure 6. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Normal mode and the LET was 53.1.

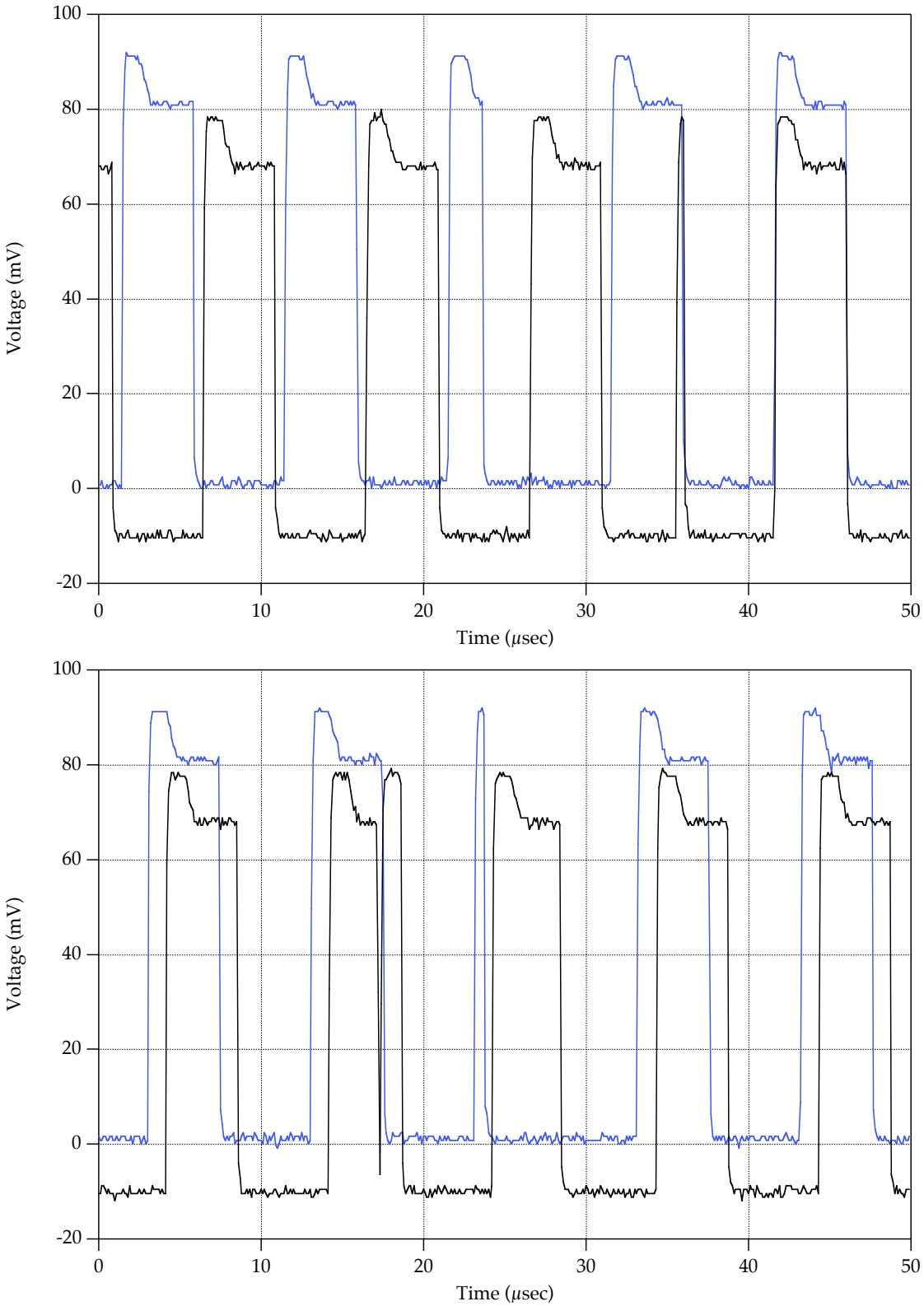


Figure 7. Sample outputs showing other unusual events when exposing the Master devices and observing the Master outputs. Operation was in Normal mode and the LET was 53.1.

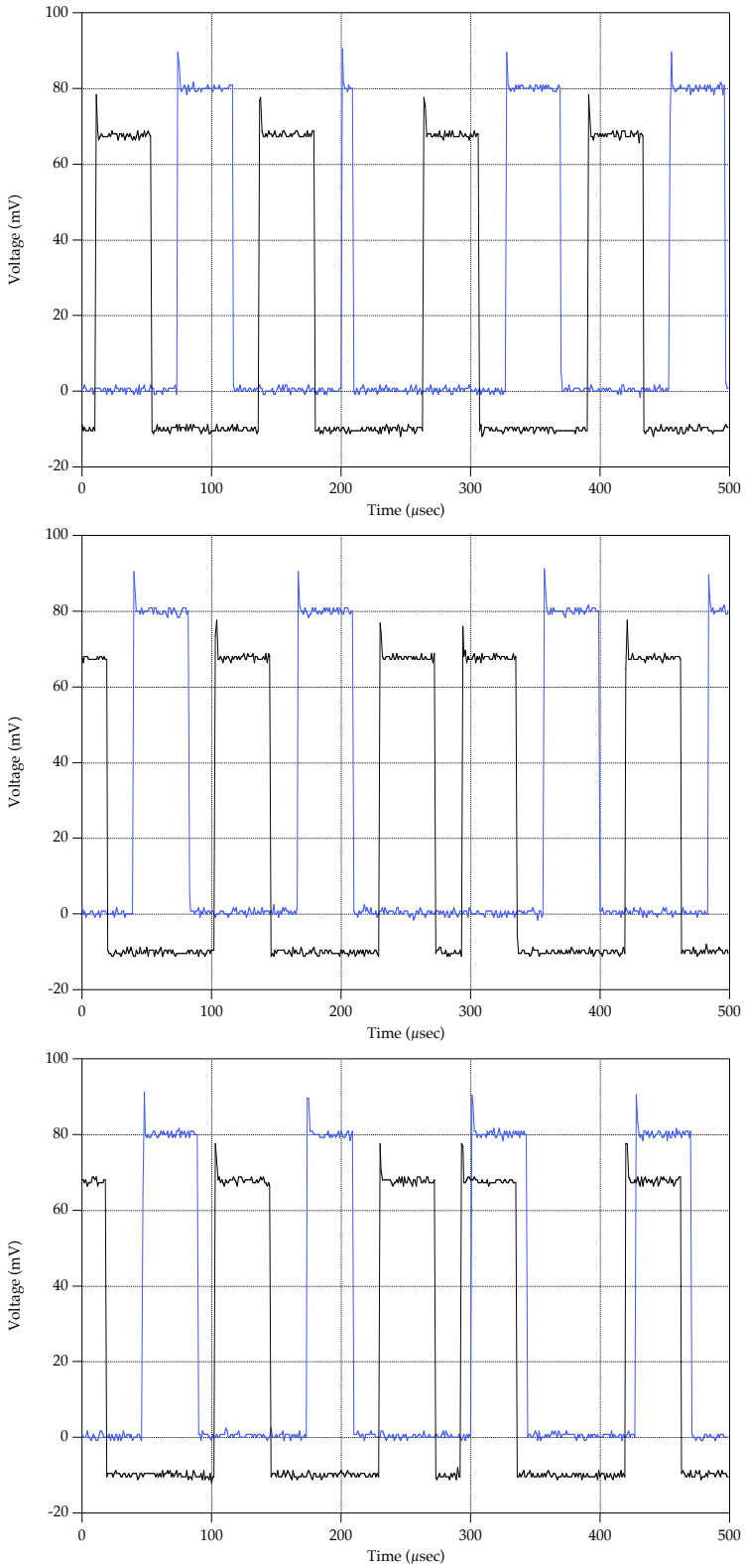


Figure 8. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Free-run mode and the LET was 8.6.

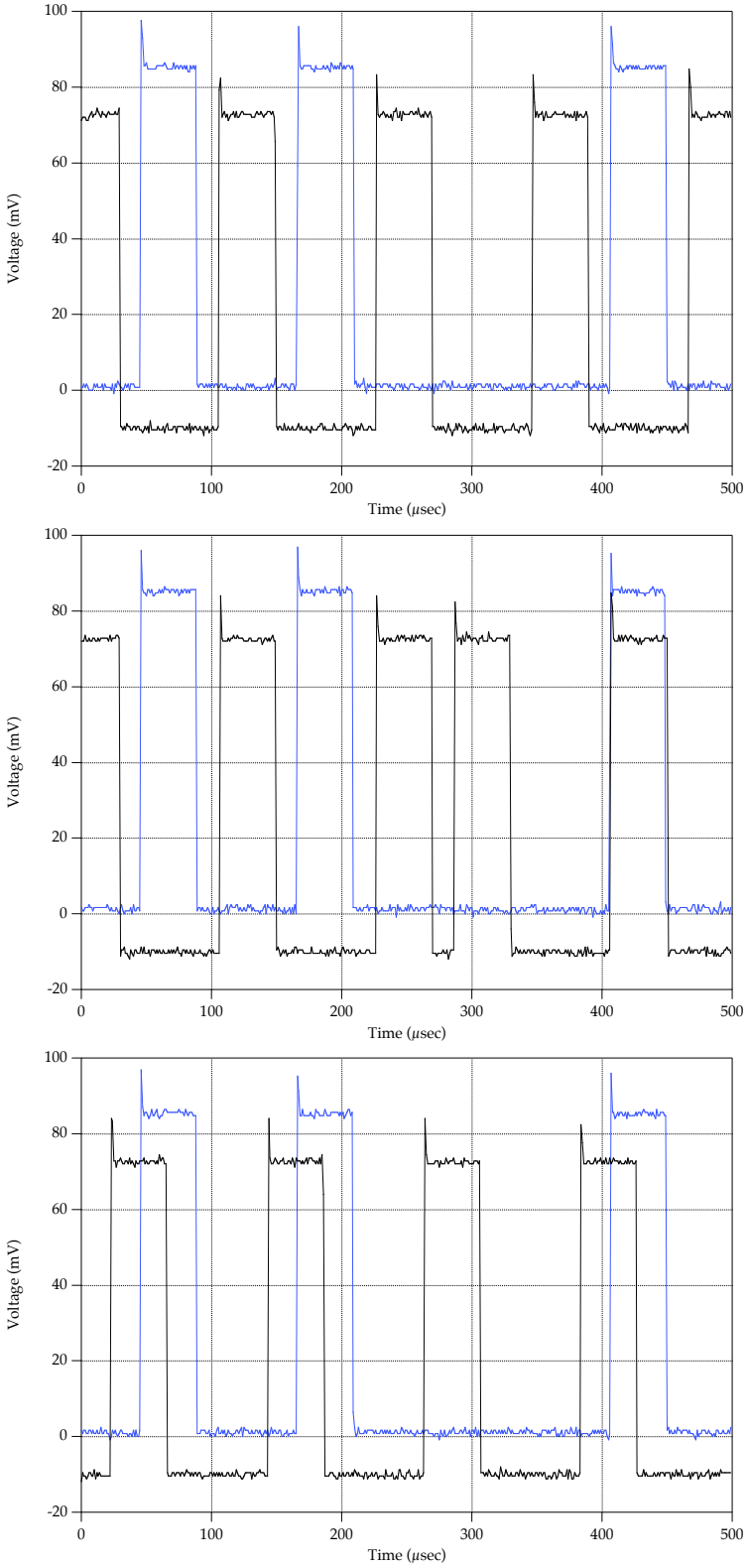


Figure 9. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Free-run mode and the LET was 28.7.

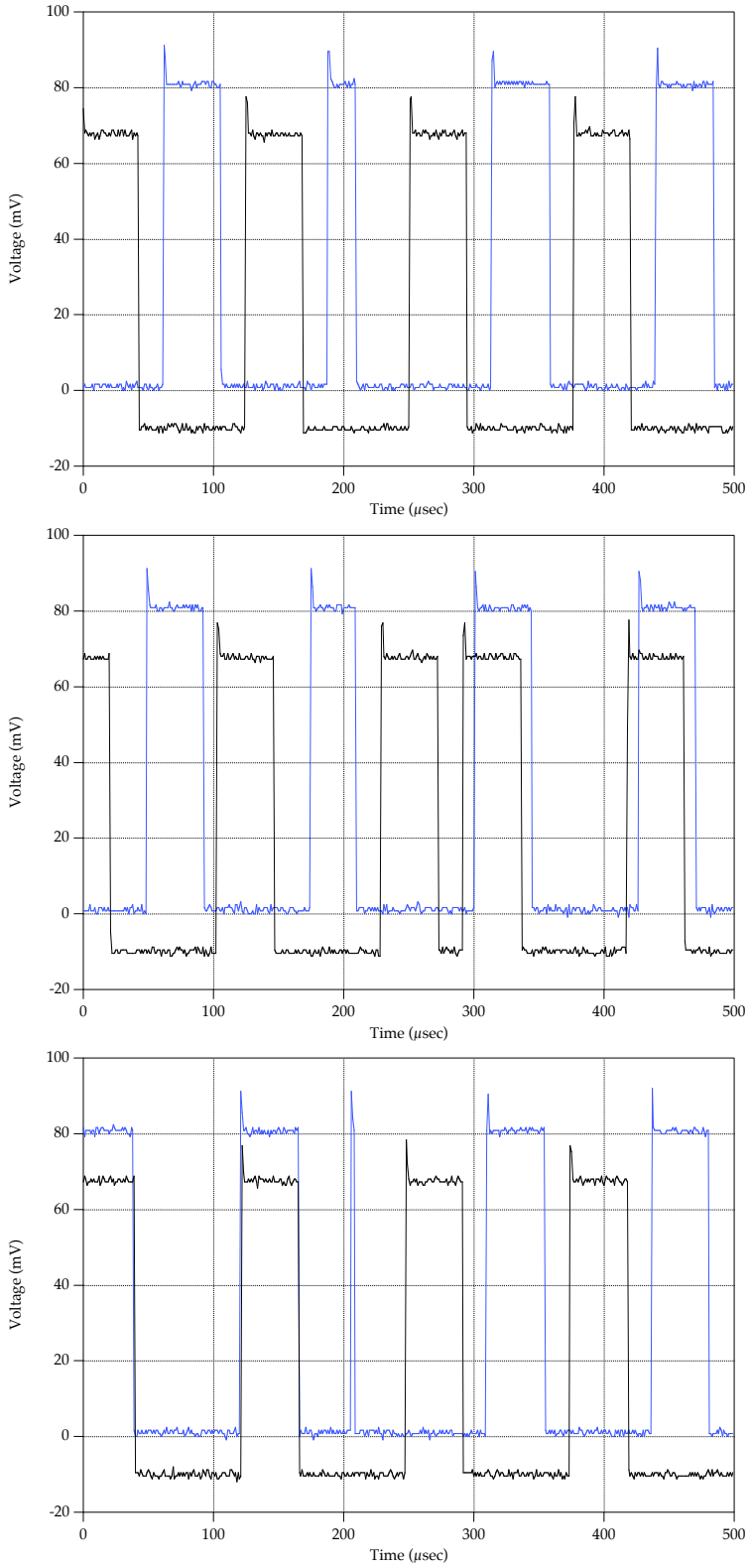


Figure 10. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Master devices and observing the Master outputs. Operation was in Free-run mode and the LET was 53.1.

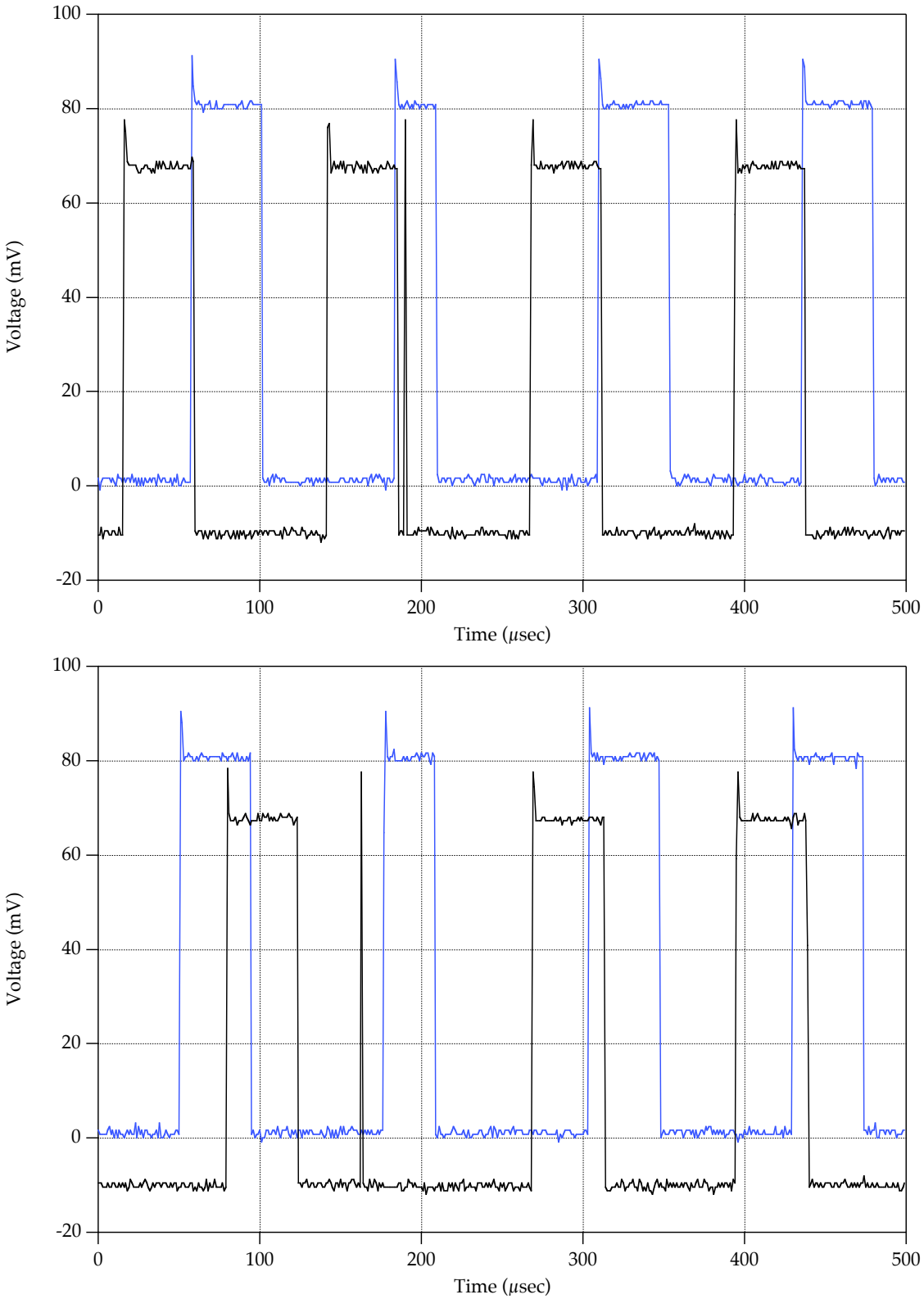


Figure 11. Sample outputs showing other unusual events when exposing the Master devices and observing the Master outputs. Operation was in Free-run mode and the LET was 53.1.

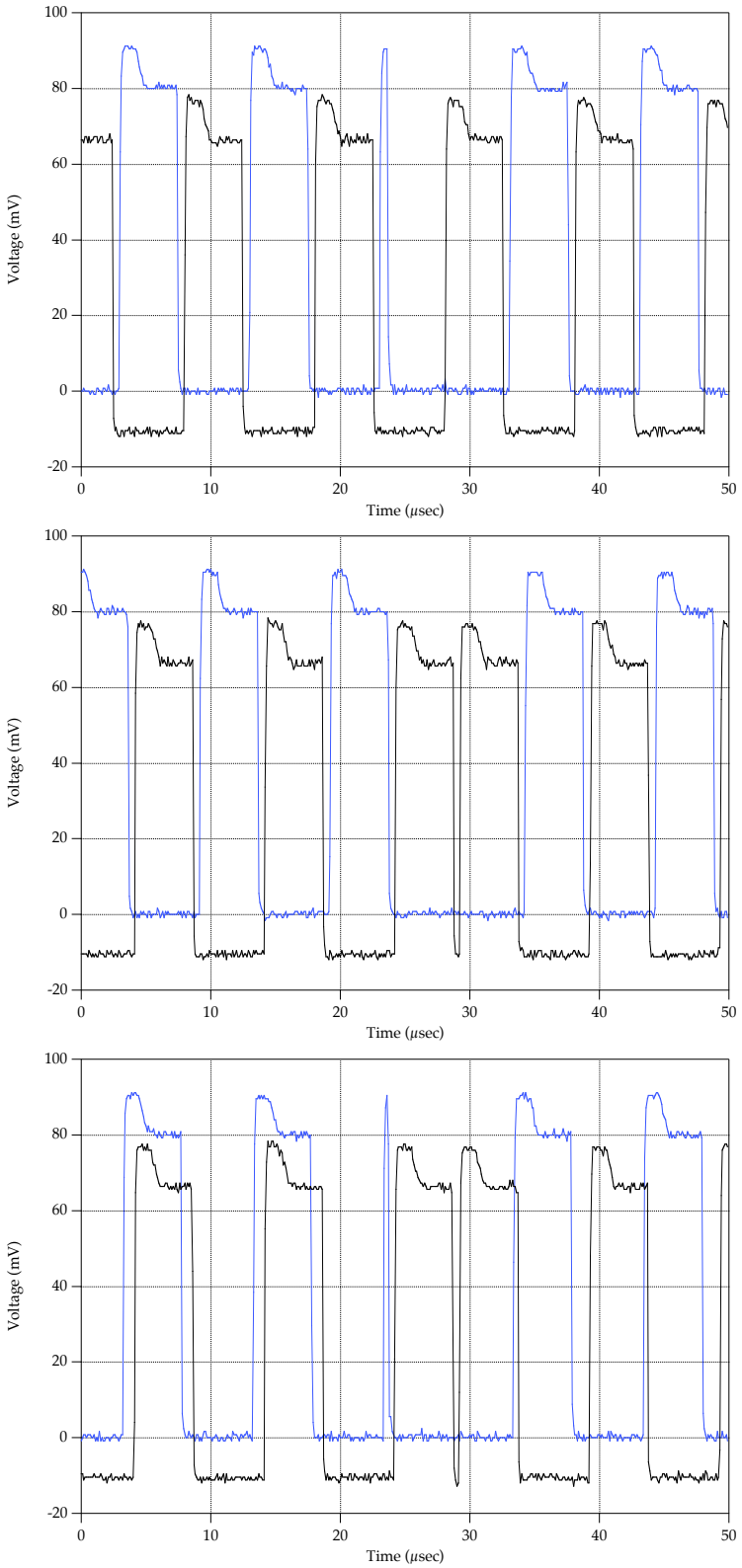


Figure 12. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Normal mode and the LET was 8.6.

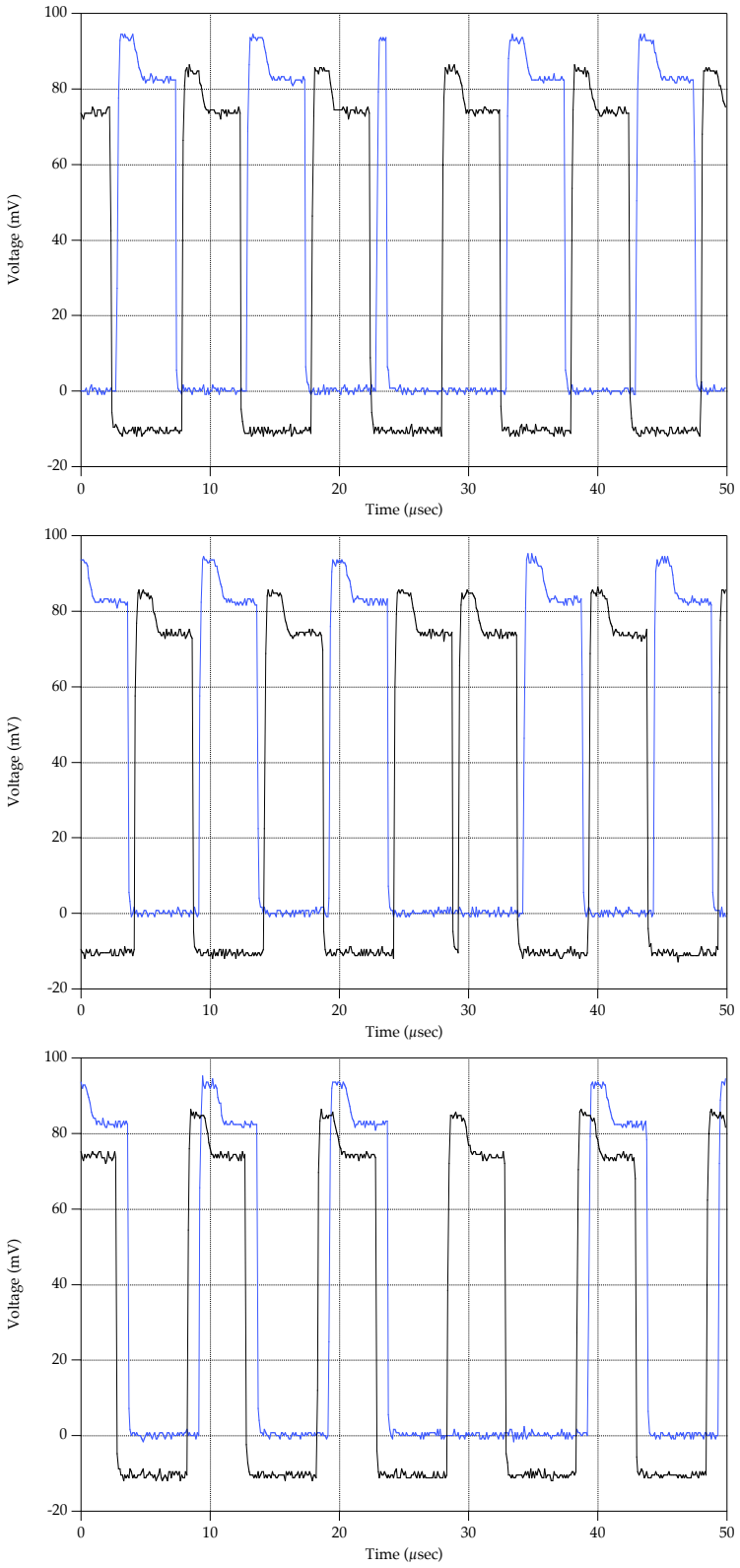


Figure 13. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Normal mode and the LET was 28.7.

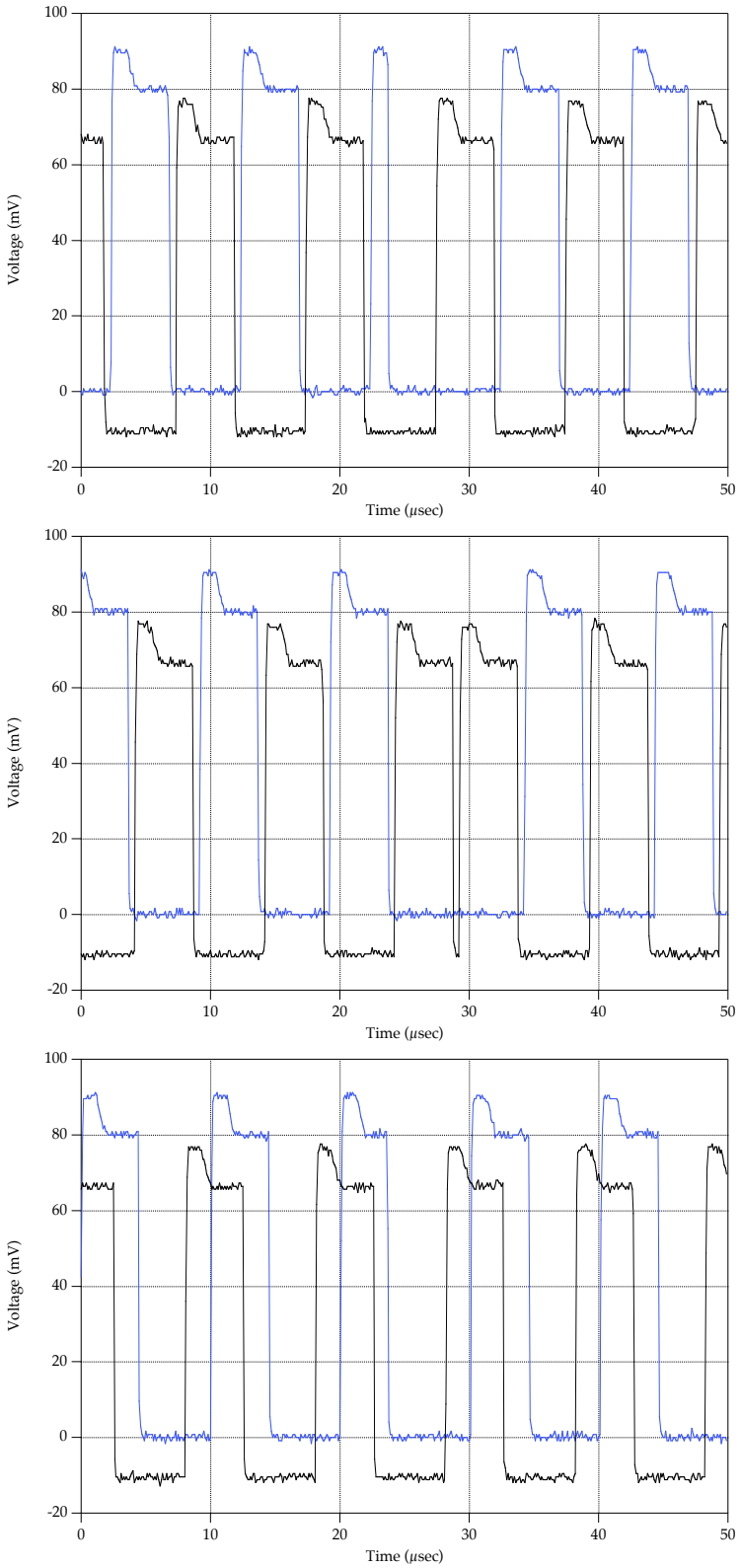


Figure 14. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Normal mode and the LET was 53.1.

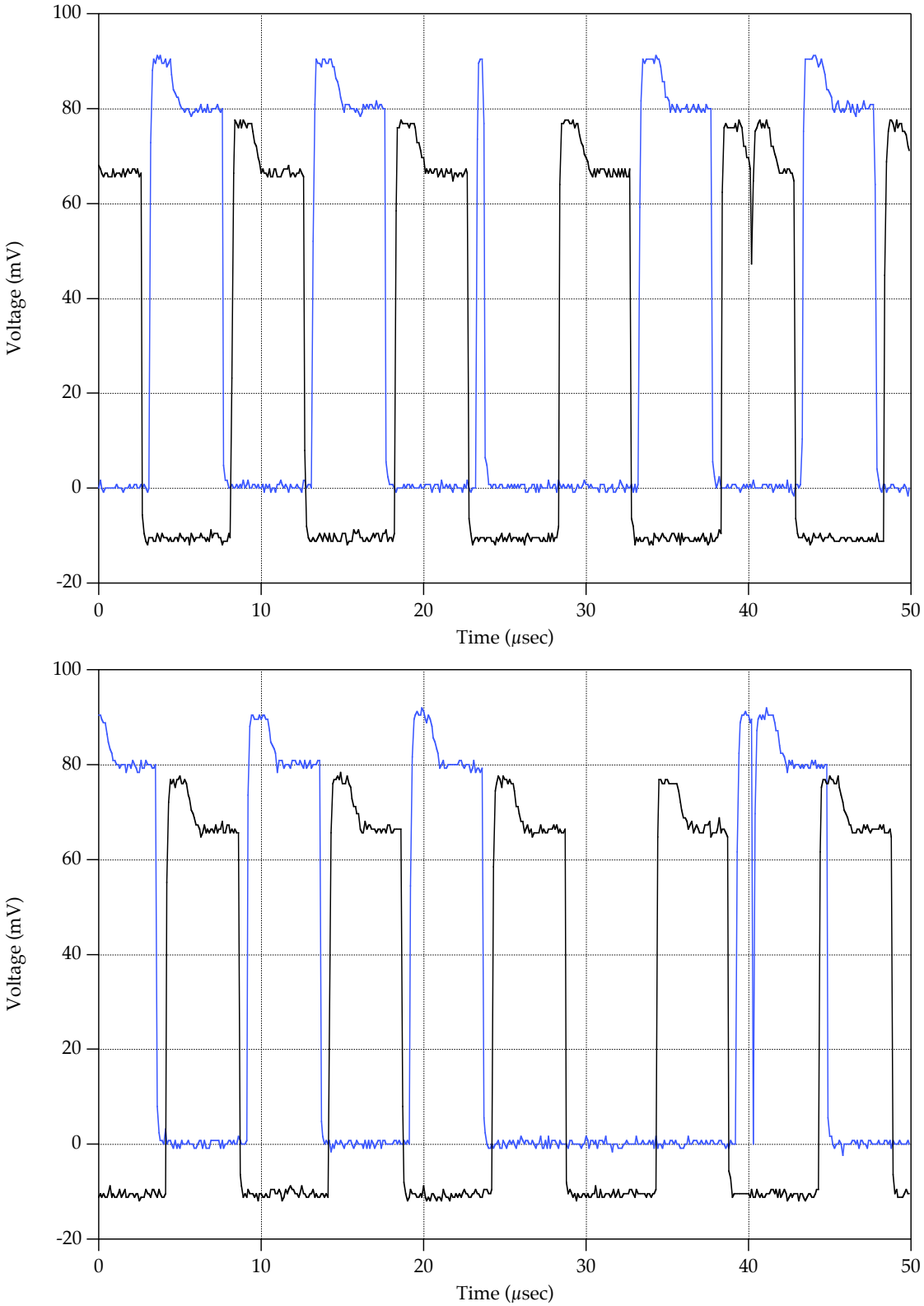


Figure 15. Sample outputs showing other unusual events when exposing the Slave devices and observing the Slave outputs. Operation was in Normal mode and the LET was 53.1.

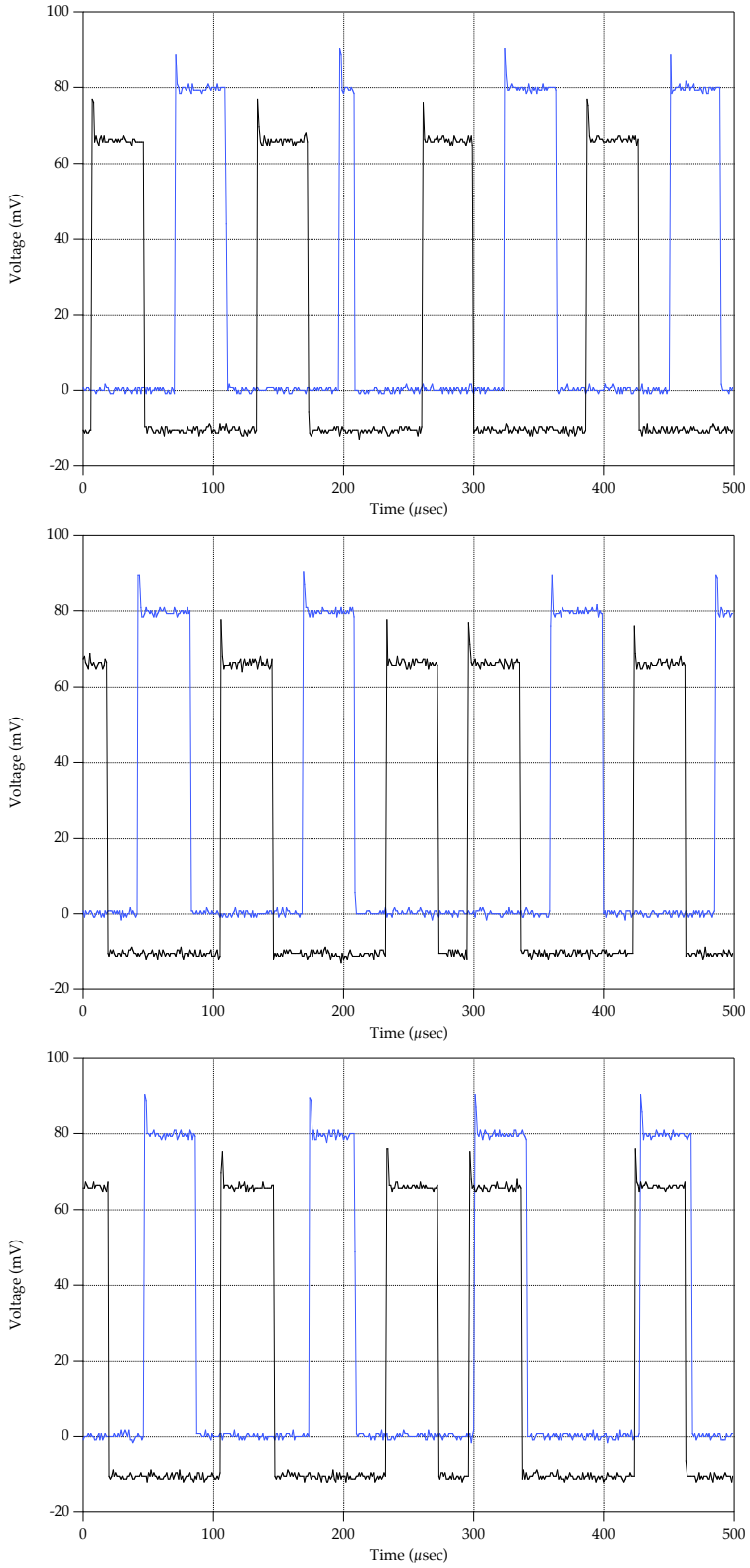


Figure 16. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Free-run mode and the LET was 8.6.

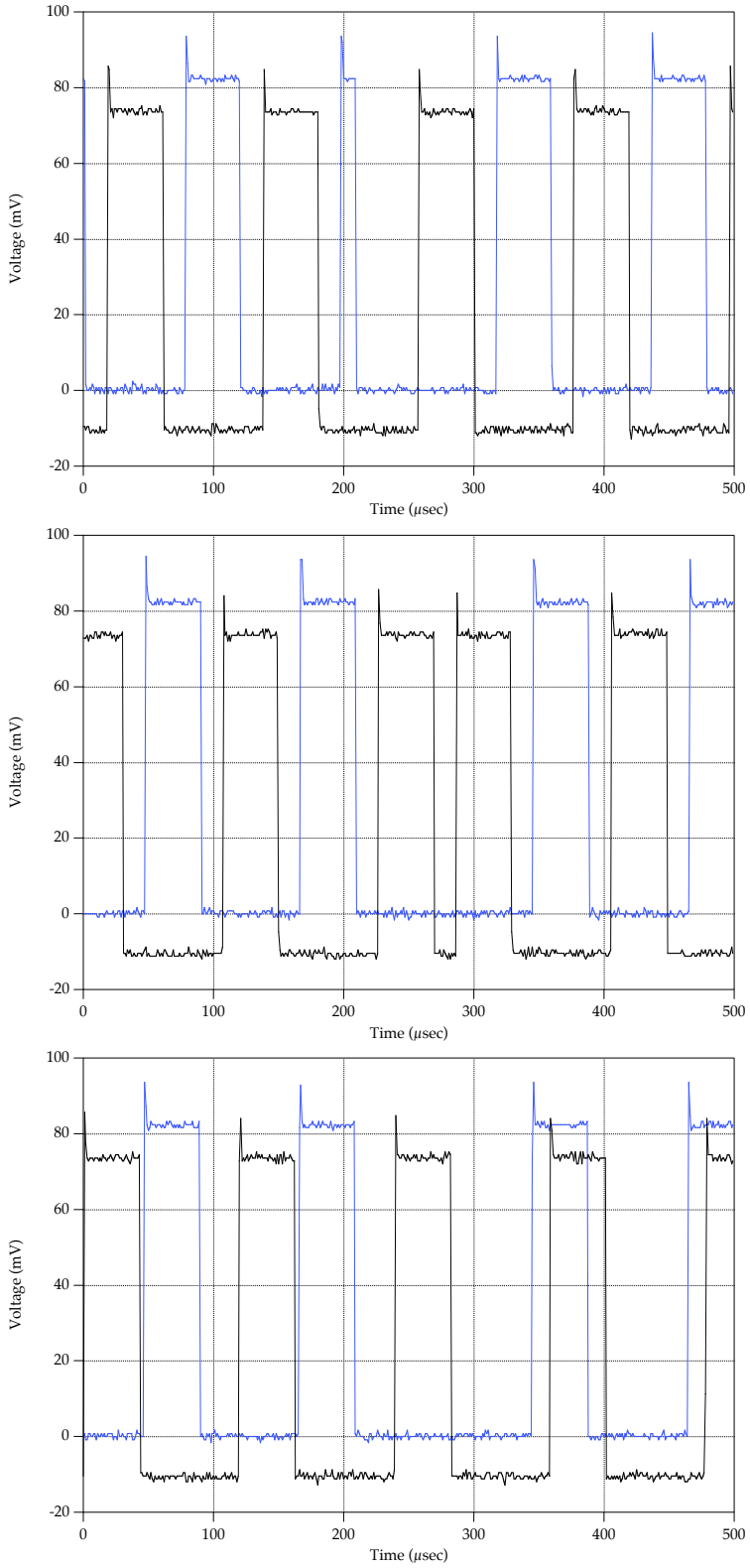


Figure 17. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Free-run mode and the LET was 28.7.

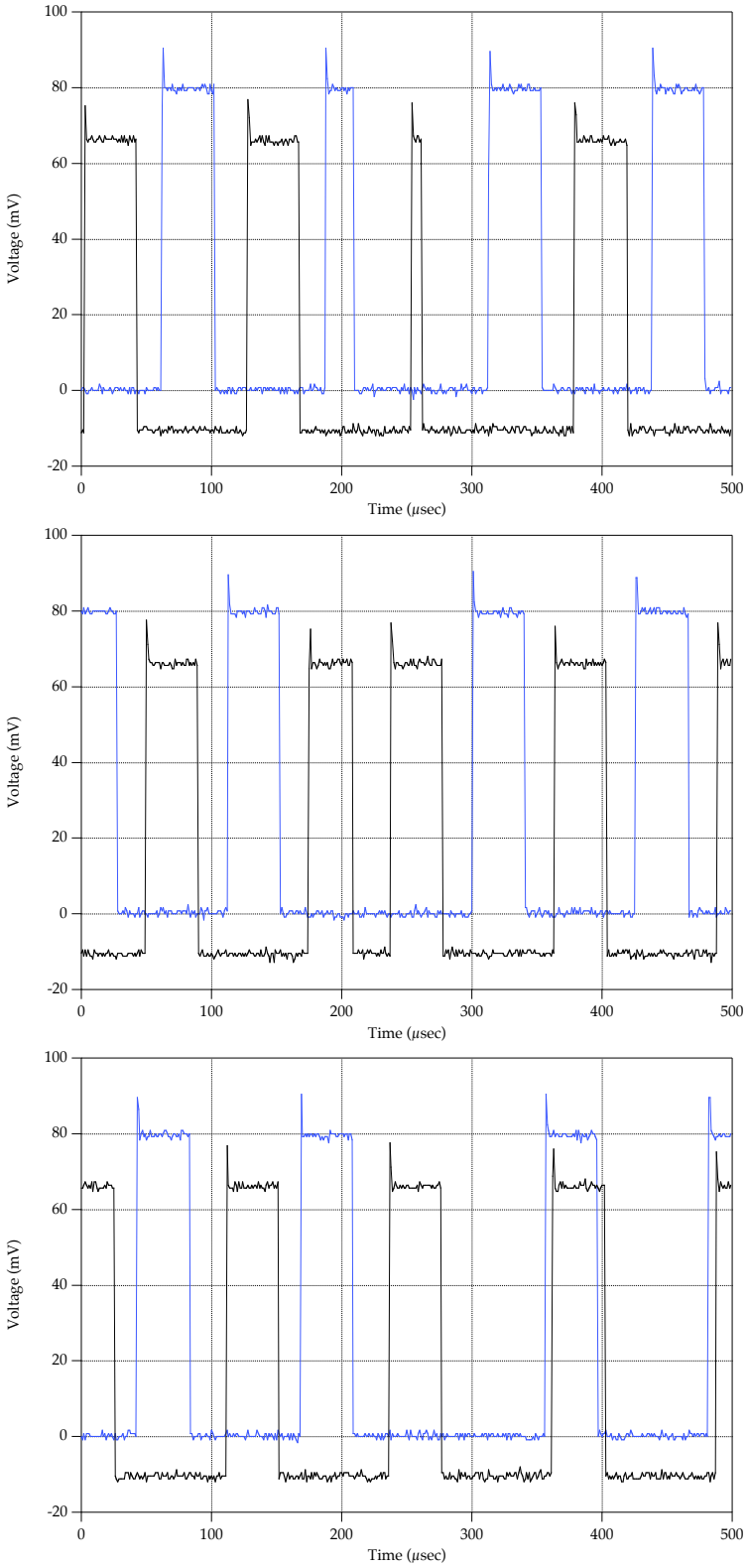


Figure 18. Sample outputs showing simple (top), double (middle), and overlapping (bottom) events when exposing the Slave devices and observing the Slave outputs. Operation was in Free-run mode and the LET was 53.1.

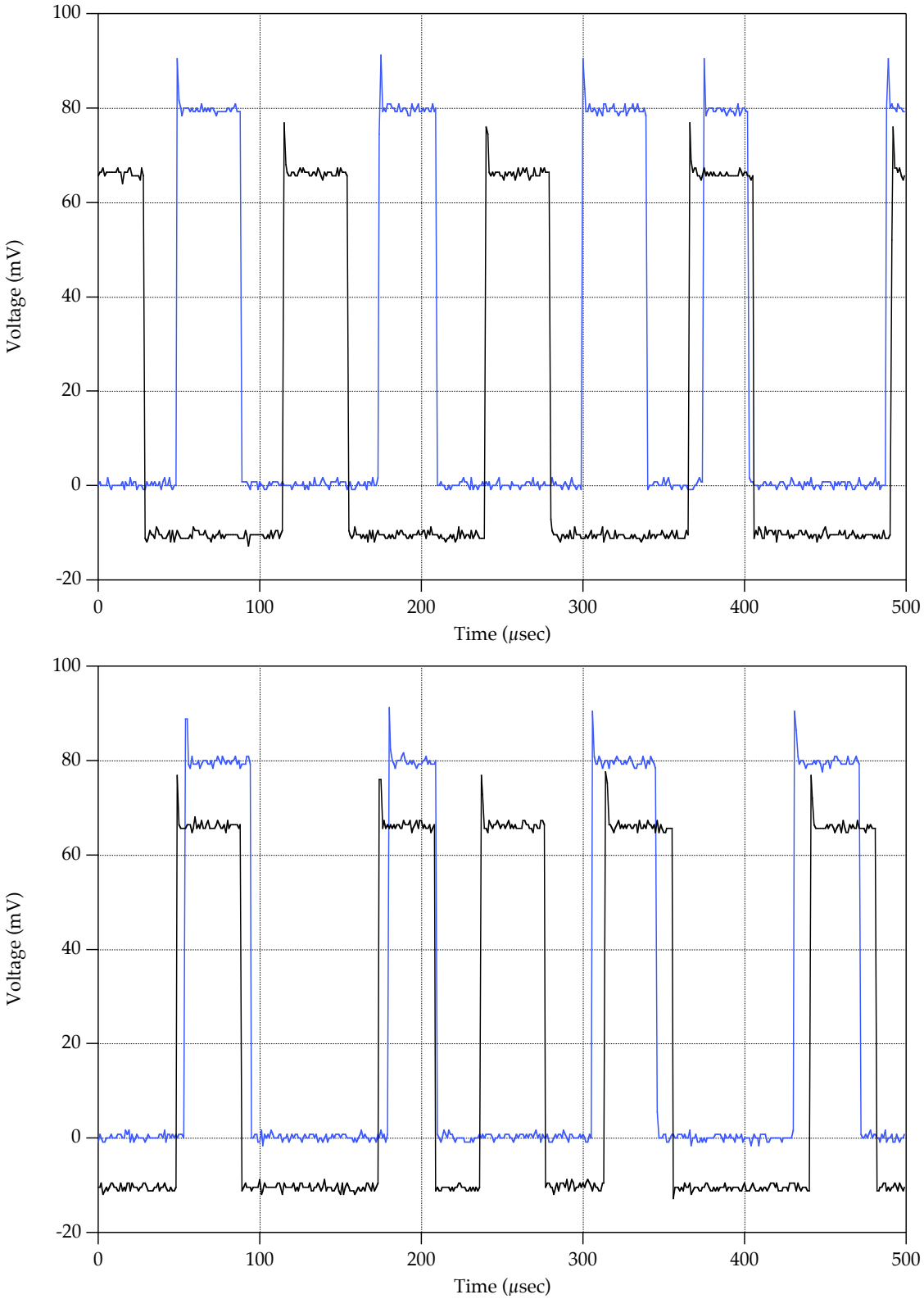


Figure 19. Sample outputs showing other unusual events when exposing the Slave devices and observing the Slave outputs. Operation was in Free-run mode and the LET was 53.1.

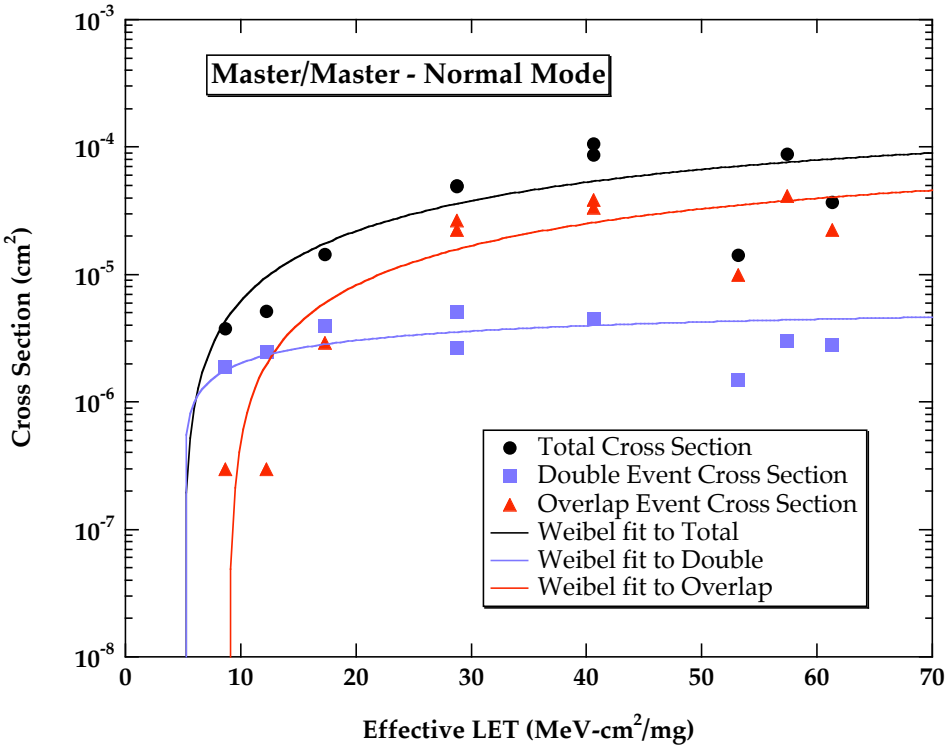


Figure 20. Cross section versus effective LET curves for the Normal mode of operation, irradiating and observing the Master device.

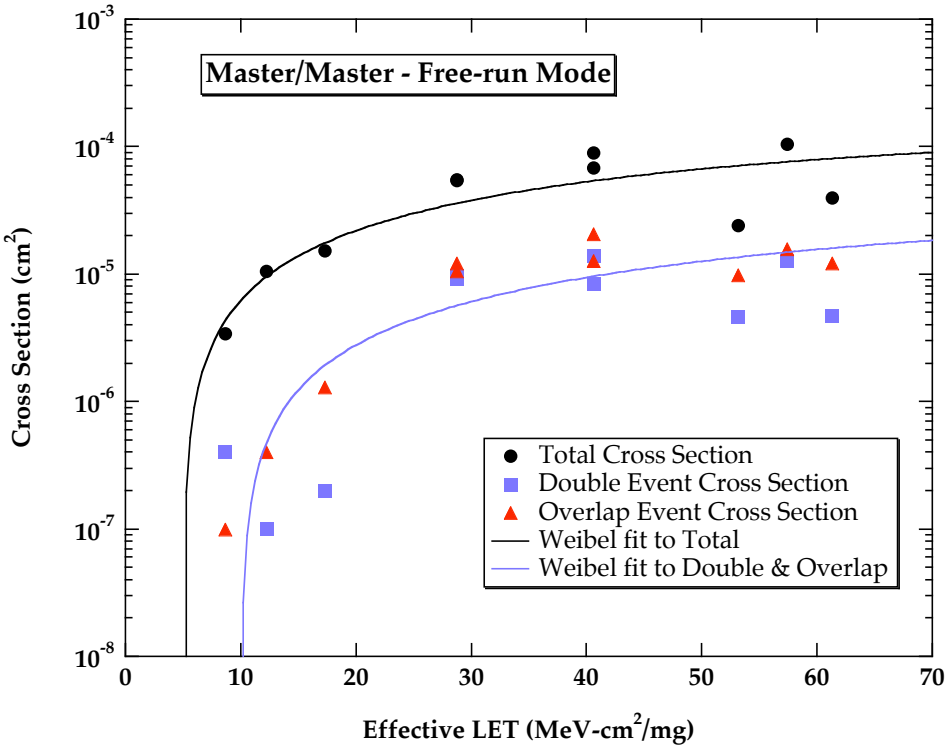


Figure 21. Cross section versus effective LET curves for the Free-run mode of operation, irradiating and observing the Master device.

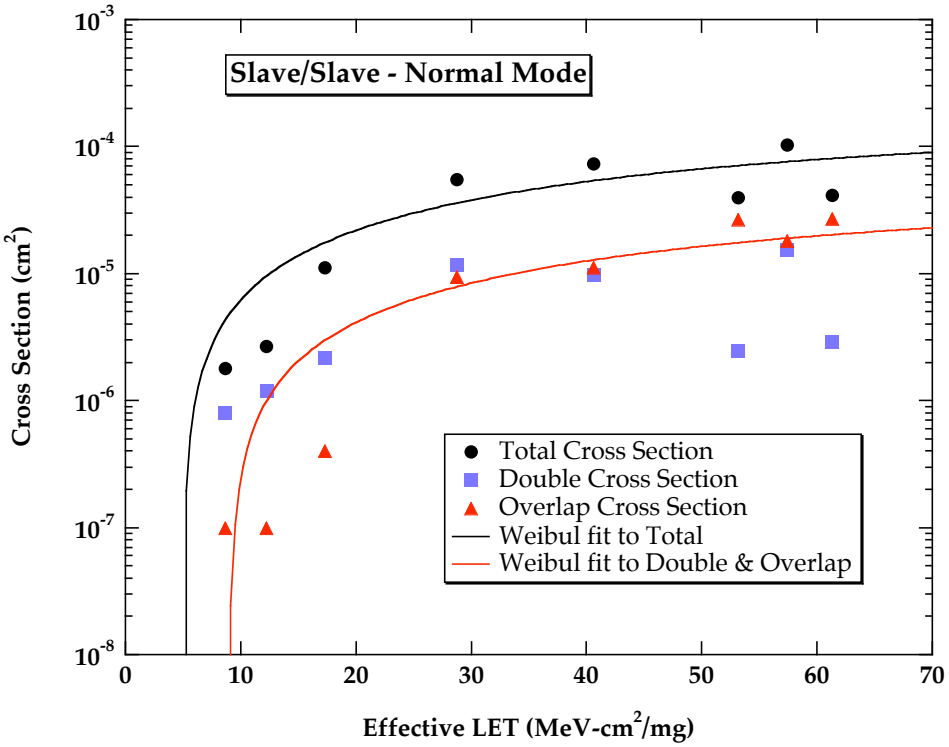


Figure 22. Cross section versus effective LET curves for the Normal mode of operation, irradiating and observing the Slave device.

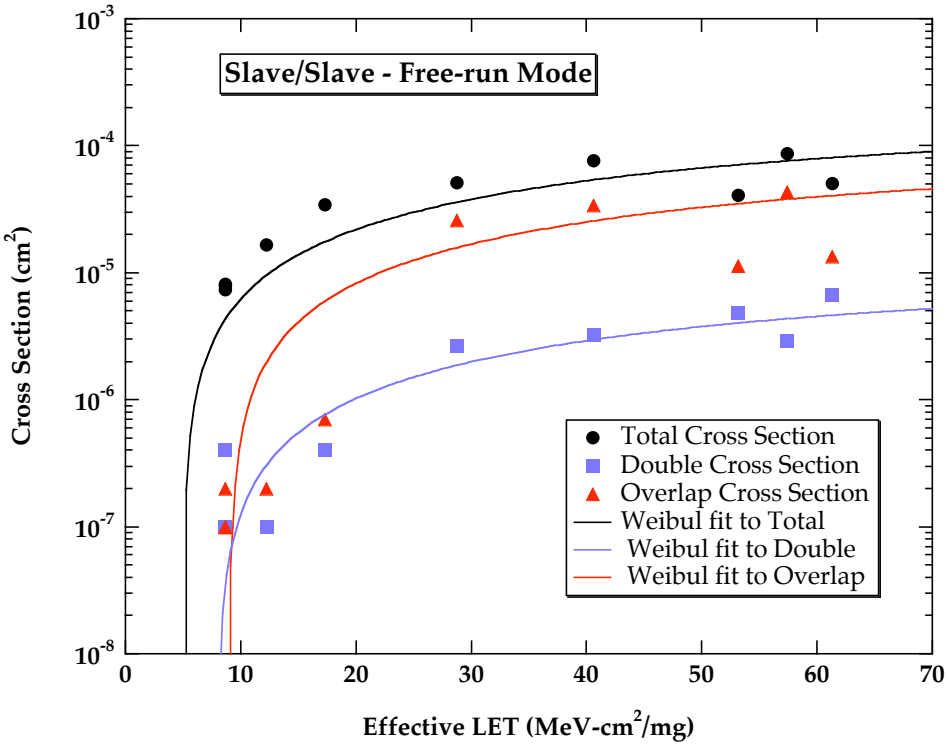


Figure 23. Cross section versus effective LET curves for the Free-run mode of operation, irradiating and observing the Slave device.

VI. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1 – Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2 – Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3 – Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4 – Not recommended for usage in any NASA/GSFC spaceflight applications.

The Linfinity SG1525A Pulse Width Modulator Controllers are currently considered Category 3 devices. If, however, the overlap events observed can lead to destructive operation and their cross section increases with addition heavy ion or proton testing, the SG1525A could become a Category 4 device.

VII. References

[1] S.H.Penzin, W.R.Crain, K.B.Crawford, S.J.Hansel and R.Koga, "The SEU in Pulse Width Modulator Controllers with Soft Start and Shutdown Circuits", 1997 IEEE Radiation Effects Data Workshop Record.

[2] S.H.Penzin, W.R.Crain, K.B.Crawford, S.J.Hansel, J.F.Kirshman and R.Koga, "Single Event Effects in Pulse Modulation Controllers", IEEE Transactions on Nuclear Science, Vol. 43, No. 6, December 1996.

[3] H.W.Johnson and M.Graham, High Speed Digital Design, a Handbook of Black Magic, 1993, Prentice Hall PTR, ISBN 0-13-395724-1.

Appendix A

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lower external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

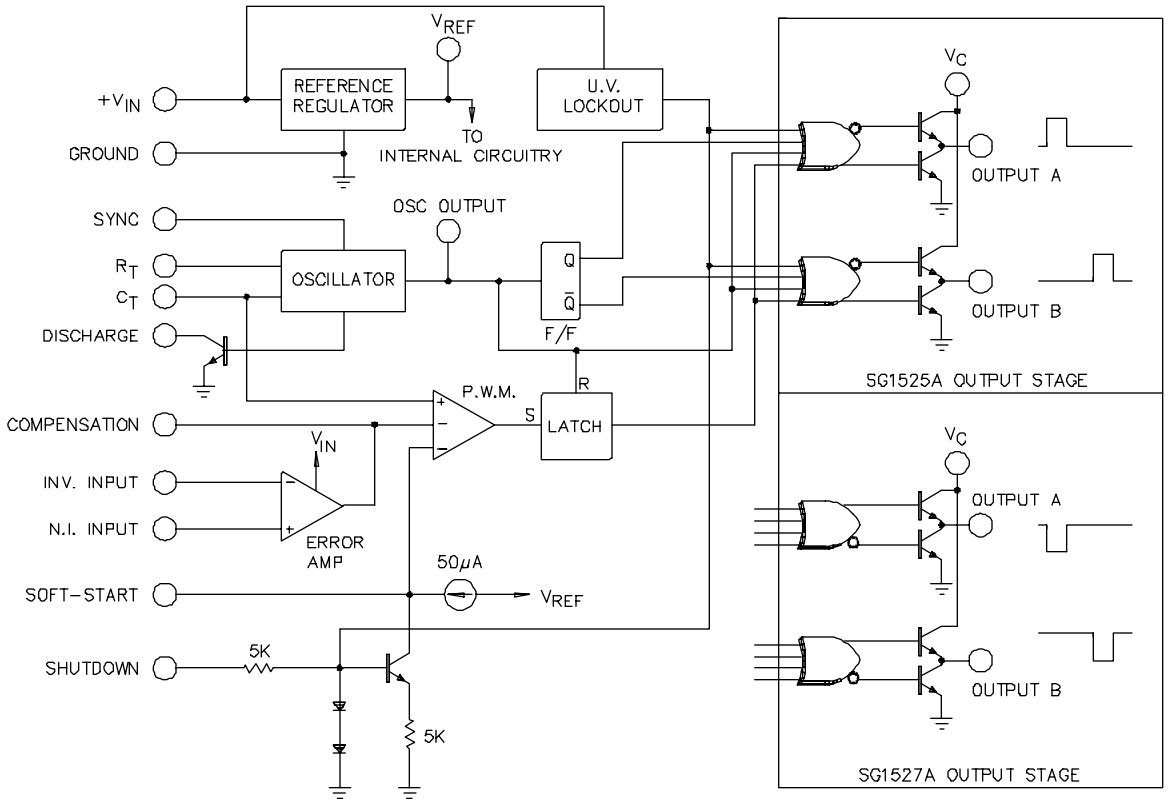
FEATURES

- **8V to 35V operation**
- **5.1V reference trimmed to ±1%**
- **100Hz to 500KHz oscillator range**
- **Separate oscillator sync terminal**
- **Adjustable deadtime control**
- **Internal soft-start**
- **Input undervoltage lockout**
- **Latching P.W.M. to prevent multiple pulses**
- **Dual source/sink output drivers**

HIGH RELIABILITY FEATURES
- SG1525A, SG1527A

- **Available to MIL-STD-883B**
- **MIL-M38510/12602BEA - JAN1525AJ**
- **MIL-M38510/12604BEA - JAN1527AJ**
- **Radiation data available**
- **LMI level "S" processing available**

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Output Current, Source or Sink 500mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature Range
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DATA

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 80°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W
L Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 65°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 8V to 35V
Collector Voltage (V_C) ..... 4.5V to 35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 350KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 150KΩ
Deadtime Resistor Range (R_D) ..... 0Ω to 500Ω
Maximum Shutdown Source Impedance 5KΩ
Oscillator Timing Capacitor (C_T) ..... 0.001µF to 0.1µF
Operating Ambient Temperature Range
  SG1525A/SG1527A ..... -55°C to 125°C
  SG2525A/SG2527A ..... -25°C to 85°C
  SG3525A/SG3527A ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1525A/SG1527A with $-55°C \le T_A \le 125°C$, SG2525A/SG2527A with $-25°C \le T_A \le 85°C$, SG3525A/SG3527A with $0°C \le T_A \le 70°C$, and $+V_{IN} = 20V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25°C$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8V$ to 35V		10	30		10	30	mV
Load Regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Temperature Stability (Note 3)	Over Operating Temperature Range		20	50		20	50	mV
Total Output Voltage Range (Note 3)	Over Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0V$, $T_J = 25°C$		80	100		80	100	mA
Output Noise Voltage (Note 3)	$10Hz \le f \le 10KHz$, $T_J = 25°C$		40	200		40	200	µVrms
Long Term Stability (Note 3)	$T_J = 125°C$		20	50		20	50	mV/khr

Note 3. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4. $F_{OSC} = 40KHz$ ($R_T = 3.6K\Omega$, $C_T = 0.01\mu F$, $R_D = 0\Omega$)
Note 5. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	37.6	40	42.4	37.6	40	42.4	KHz
Voltage Stability	V_{IN} = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 3)	MIN ≤ T_J ≤ MAX		±3	±6		±3	±6	%
Minimum Frequency (Note 3)	R_T = 150KΩ, C_T = 0.1µF			150			150	Hz
Maximum Frequency (Note 3)	R_T = 2KΩ, C_T = 1nF	350			350			KHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		V
Clock Width	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	60	75		60	75		dB
Gain-Bandwidth Product (Note 3)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	50	60		50	60		dB
P.W.M. Comparator Section								
Minimum Duty Cycle	V_{COMP} = 0.6V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Input Threshold (Note 4)	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current			.05	2.0		.05	2.0	µA
Soft-Start Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Output Drivers Section (each transistor, V_C = 20V)								
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.2		1.0	2.2	V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
Collector Leakage (Note 5)	V_C = 35V			200			200	µA
Rise Time	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Shutdown Delay (Note 3)	V_{SD} = 3V, C_S = 0, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Total Standby Current								
Standby Current	V_{IN} = 35V		14	20		14	20	mA

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OSCILLATOR SECTION

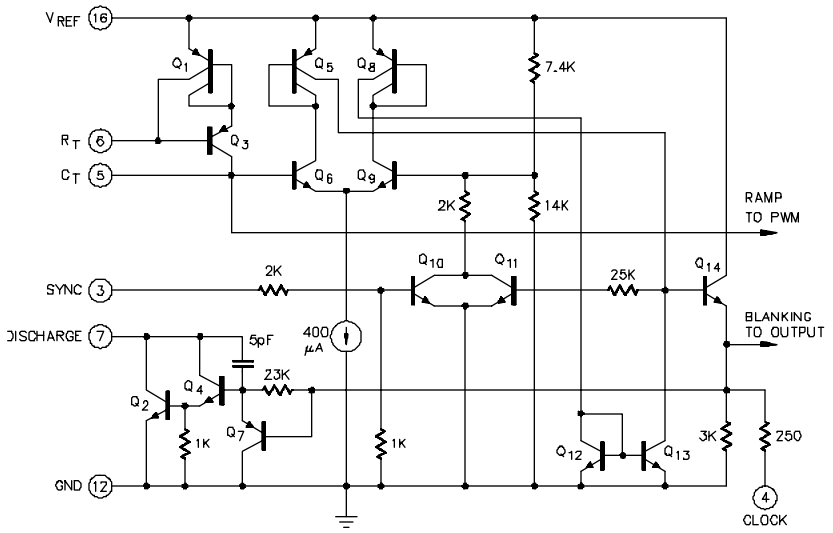

FIGURE 1 - OSCILLATOR SCHEMATIC

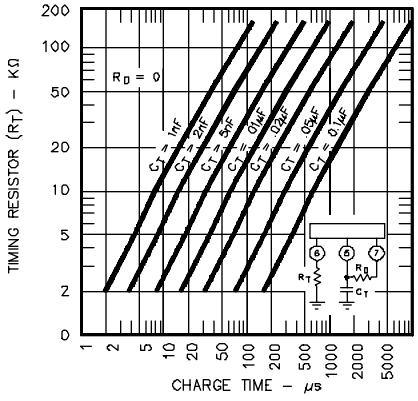

FIGURE 2 - OSCILLATOR CHARGE TIME VS. R_T AND C_T

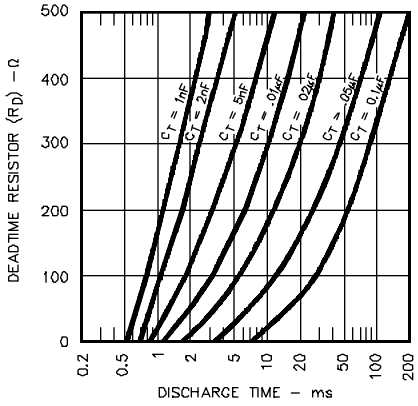

FIGURE 3 - OSCILLATOR DISCHARGE TIME VS. R_D AND C_T

ERROR AMPLIFIER SECTION

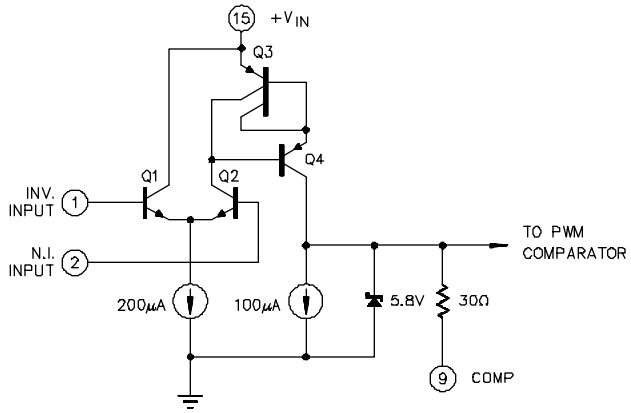

FIGURE 4 - ERROR AMPLIFIER

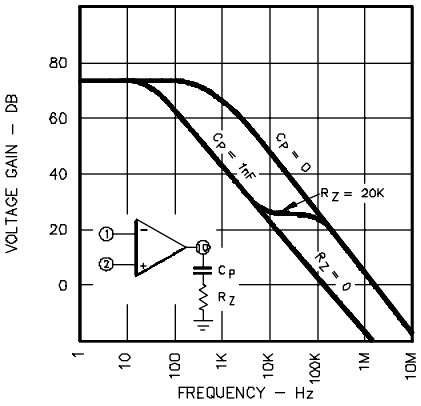

FIGURE 5 - ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

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OUTPUT SECTION

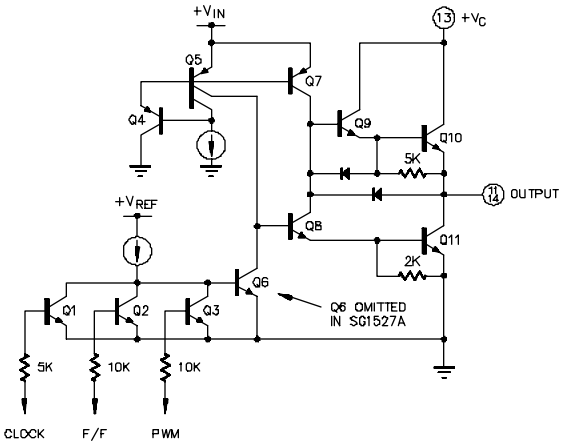


FIGURE 6 -OUTPUT CIRCUIT (½ Circuit Shown)

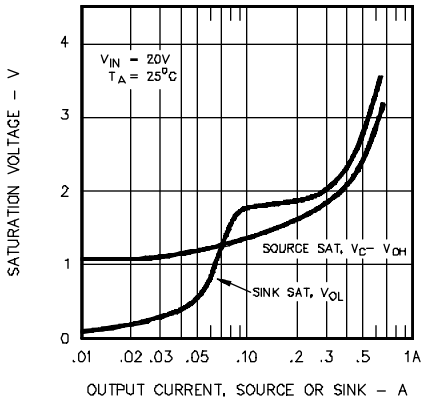
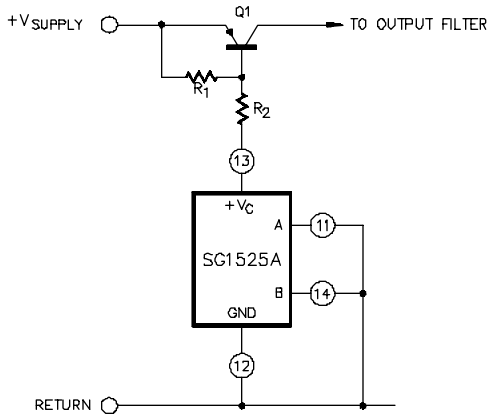
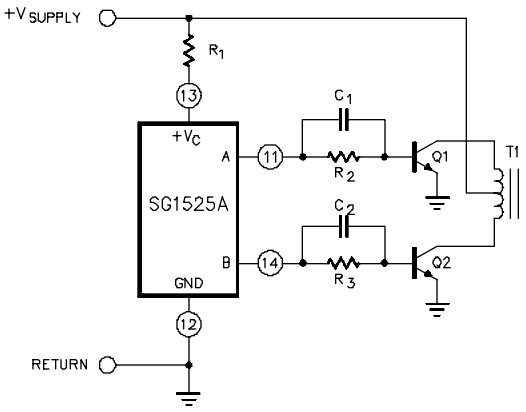


FIGURE 7 - OUTPUT SATURATION CHARACTERISTICS

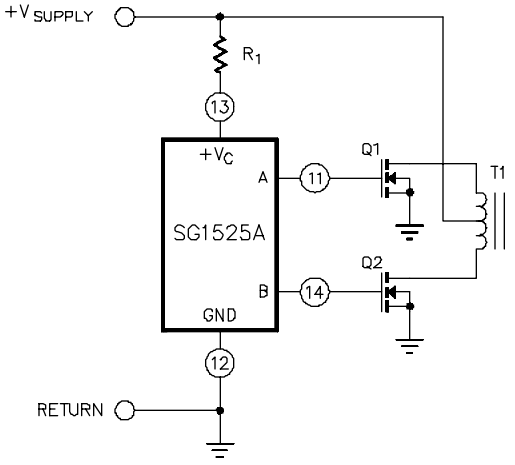
APPLICATION INFORMATION



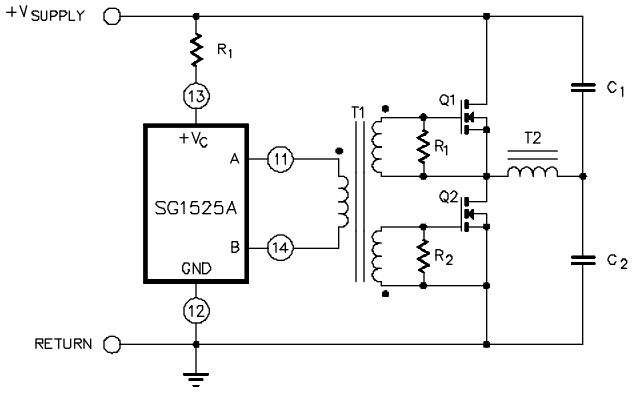
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3 . Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

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APPLICATION INFORMATION (continued)

SHUTDOWN OPTIONS

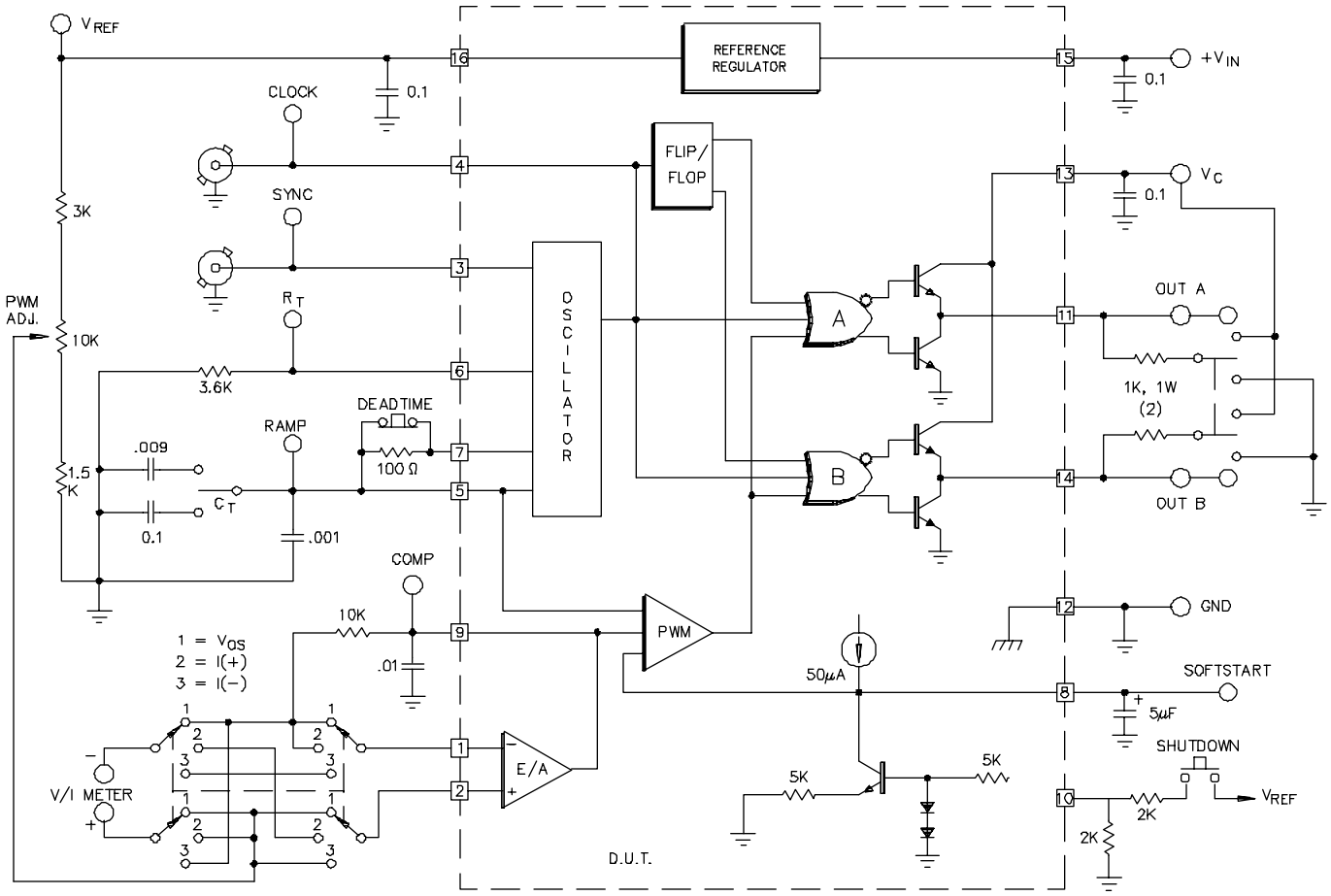
1. Use an external transistor or open-collector comparator to pull down on the Comp terminal. This will set the PWM latch turning off both outputs. If the shutdown signal is momentary, pulse-by-pulse protection can be accomplished as the PWM latch will be reset with each clock pulse.

2. The same results can be accomplished by pulling down on the Soft-Start terminal with the difference that on this pin, shutdown will not affect the amplifier compensation network but must discharge any Soft-Start capacitor.

3. Apply a positive-going signal to the Shutdown terminal. This will provide most rapid shutdown of the outputs but will not immediately set the PWM latch if there is a Soft-Start capacitor. This capacitor will discharge but with a current of approximately twice the charging current.

4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Soft-Start terminal. Slow turn-on may still be accomplished by applying an external capacitor, blocking diode, and charging resistor to the comp terminal. (See SG1524 Application Note).

SG1525A/1527A LAB TEST FIXTURE



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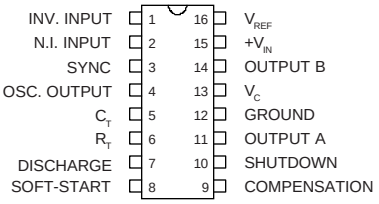
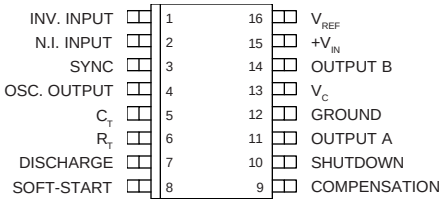
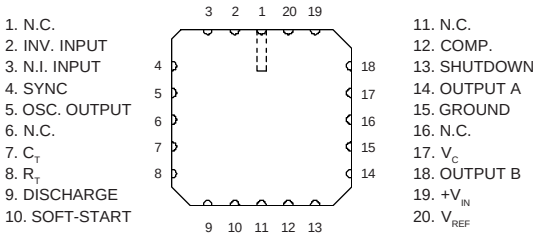
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1525AJ/883B JAN1525AJ SG1525AJ/DESC SG1525AJ SG2525AJ SG3525AJ SG1527AJ/883B JAN1527AJ SG1527AJ/DESC SG1527AJ SG2527AJ SG3527AJ	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2525AN SG3525AN SG2527AN SG3527AN	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2525ADW SG3525ADW SG2527ADW SG3527ADW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1525AL/883B SG1525AL SG1527AL/883B SG1527AL	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

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Appendix B

Bandwidth of the probe will be proportional to the rise time of the probe. Any usual measure of rise time will do, though the proportionality factor peculiar to each will vary slightly. The 10-90% rise time is used here. Two 10-90% rise times (time to rise from a minimum to the maximum and back) approximately equals one cycle of the frequency at which the magnitude is 80% of nominal.

The composite 10-90% rise time of this type of probe consists of the RSS of three components' rise time: the connections, the coax and the sense-loop diameter.

Connections consist of two connectors (one at each end of the 15' coax). These are twist-on BNCs each with a 10-90% rise time of 0.022 ns. These connectors will add rise times with the other components. The 15-foot lengths of RG-58 coaxial cable have a rise time value of approximately 0.4 ns. The sense loop diameter was well under 1", giving a rise time of less than 0.17 ns.

The combined rise time of these is:

(2(0.022)^2 + (0.4)^2 + (0.17)^2)^0.5 =
(.000968 + 0.16 + .0289)^0.5 =
0.4357 ns

This corresponds to a bandwidth of greater than 1 GHz. The actual rise time of the signal, which is in itself a combination of the signal rise time and the probe and scope rise times, was seen to be on the order of 0.2 us, a factor of 500 slower than the conservatively calculated probe rise time. It is thus assumed that the probe bandwidth does not affect the captured signal integrity.

Appendix C

PD - 93789A

International
IOR Rectifier

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-39)

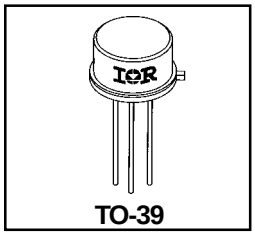
IRHF57130

100V, N-CHANNEL

R5™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHF57130	100K Rads (Si)	0.08Ω	11.7A
IRHF53130	300K Rads (Si)	0.08Ω	11.7A
IRHF54130	600K Rads (Si)	0.08Ω	11.7A
IRHF58130	1000K Rads (Si)	0.10Ω	11.7A



TO-39

International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low $R_{DS(on)}$
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Ratings
- Dynamic dv/dt Ratings
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	11.7	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	7.4	
I_{DM}	Pulsed Drain Current ①	47	
P_D @ T_C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	173	mJ
I_{AR}	Avalanche Current ①	11.7	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.9	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063 in./1.6mm from case for 10s)	
	Weight	0.98 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.12	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.08	Ω	V_{GS} = 12V, I_D = 7.4A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	8.7	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 7.4A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS}= 80V ,V_{GS}=0V
		—	—	25		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	50	nC	V_{GS} =12V, I_D = 11.7A
Q_{gs}	Gate-to-Source Charge	—	—	7.4		V_{DS} = 50V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	20		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 50V, I_D = 11.7A
t_r	Rise Time	—	—	100		R_G = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
t_f	Fall Time	—	—	30		
$L_S + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	1038	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	362	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	45	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	11.7	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	47		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_j = 25°C, I_S = 11.7A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	202	ns	T_j = 25°C, I_F = 11.7A, di/dt ≥ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	982	µC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175		Typical socket mount

Note: Corresponding Spice and Saber models are available on the G&S Website.
For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 600K Rads(Si)[1]		1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage ④	2.0	4.0	1.5	4.0		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	—	10	µA	V_{DS}= 80V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.064	—	0.08	Ω	V_{GS} = 12V, I_D =7.4A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.08	—	0.10	Ω	V_{GS} = 12V, I_D =7.4A
V_{SD}	Diode Forward Voltage ④	—	1.5	—	1.5	V	V_{GS} = 0V, I_S = 11.7A

1. Part numbers IRHF57130, IRHF53130 and IRHF54130
2. Part number IRHF58130

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V) @V_{GS}=0V	@V_{GS}=-5V	@V_{GS}=-10V	@V_{GS}=-15V	@V_{GS}=-20V
Br	36.7	309	39.5	100	100	100	100	100
I	59.8	341	32.5	100	100	100	35	25
Au	82.3	350	28.4	100	100	80	25	—

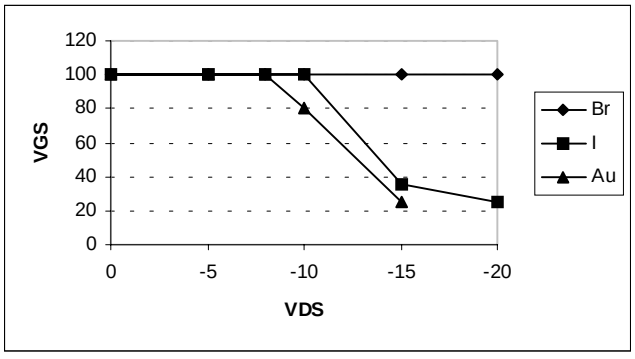


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

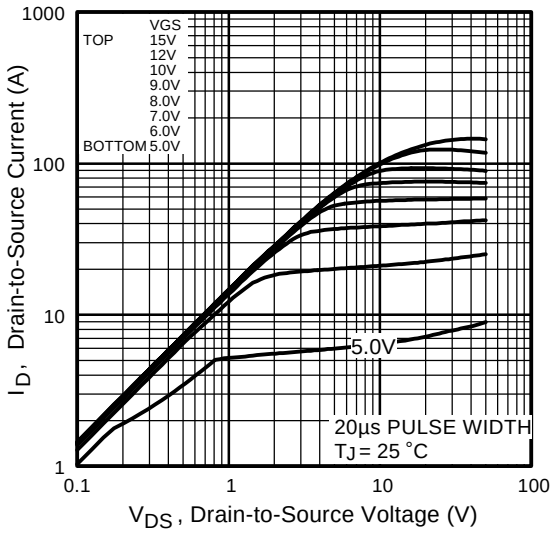


Fig 1. Typical Output Characteristics

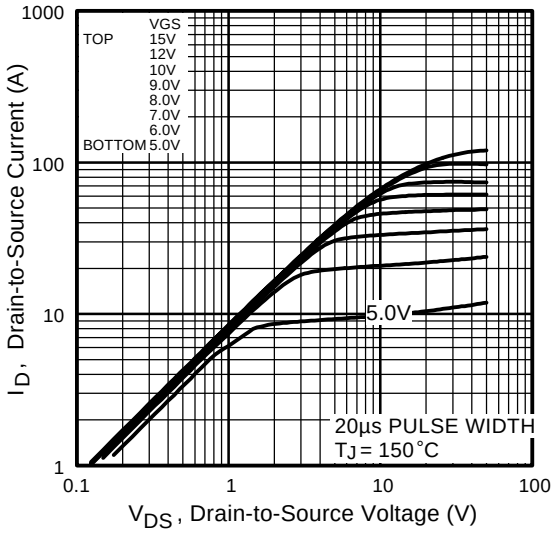


Fig 2. Typical Output Characteristics

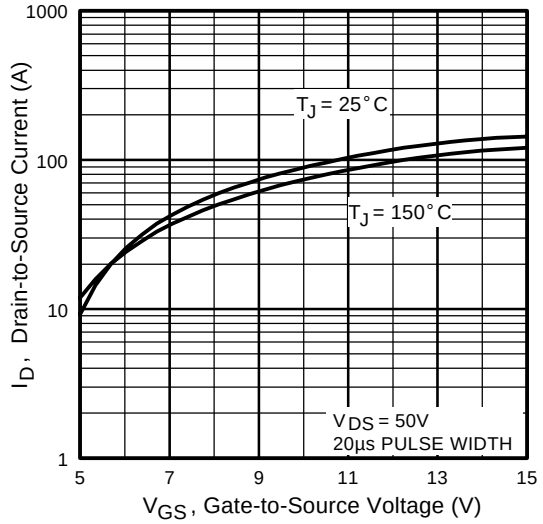


Fig 3. Typical Transfer Characteristics

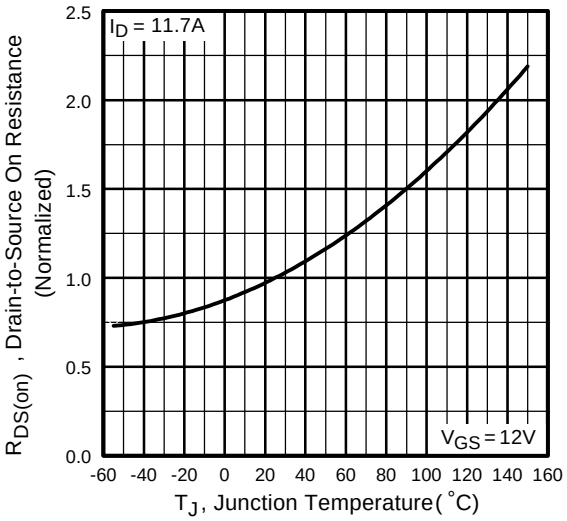


Fig 4. Normalized On-Resistance Vs. Temperature

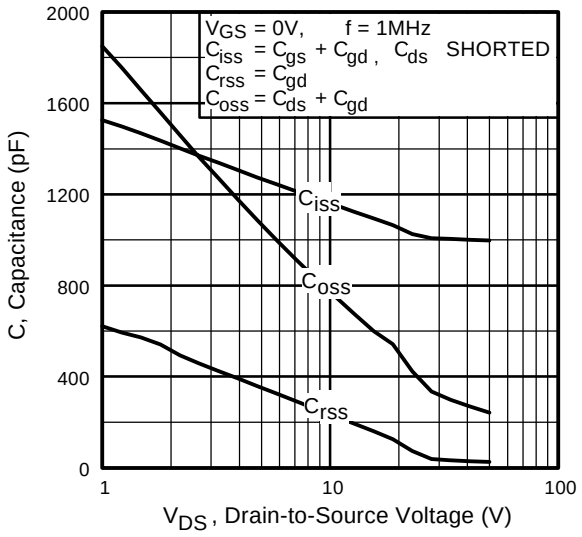


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

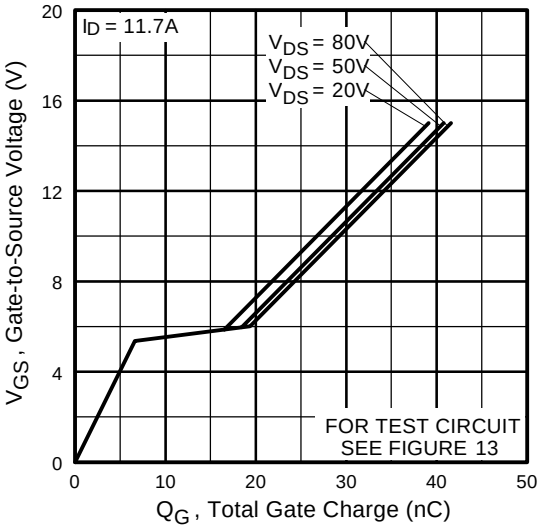


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

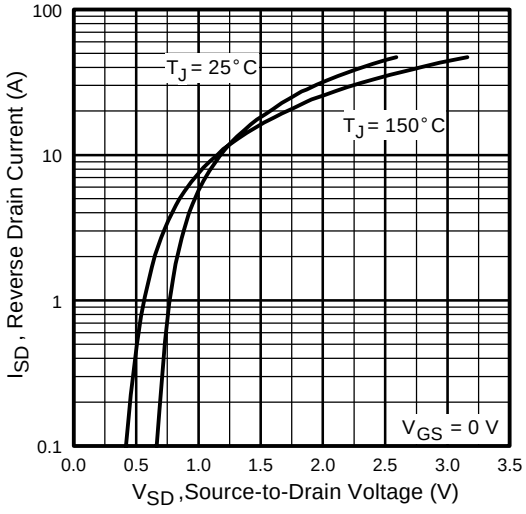


Fig 7. Typical Source-Drain Diode Forward Voltage

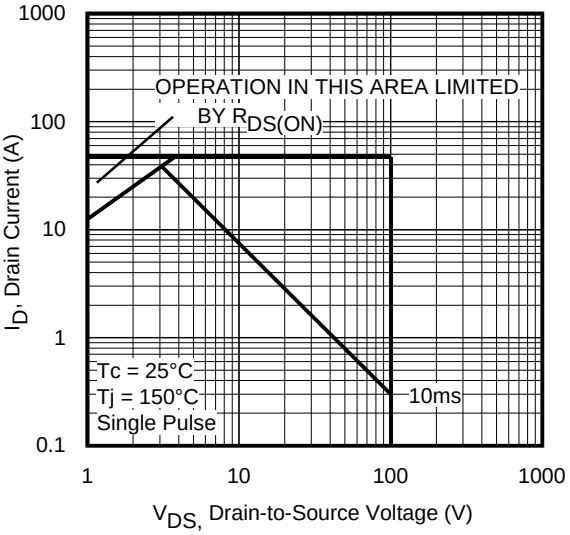


Fig 8. Maximum Safe Operating Area

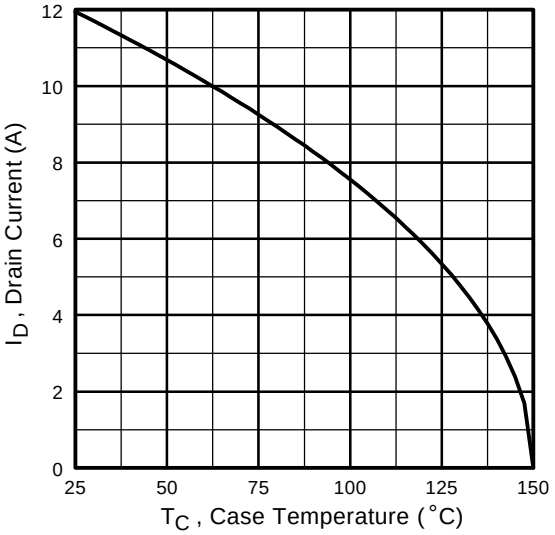


Fig 9. Maximum Drain Current Vs. Case Temperature

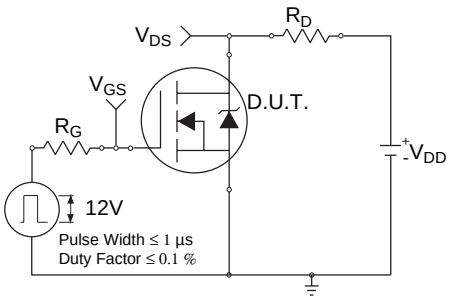


Fig 10a. Switching Time Test Circuit

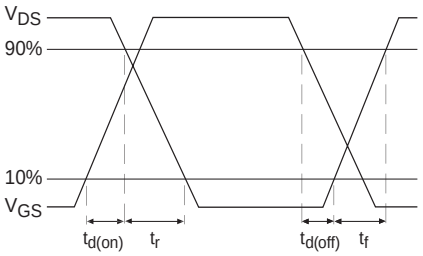


Fig 10b. Switching Time Waveforms

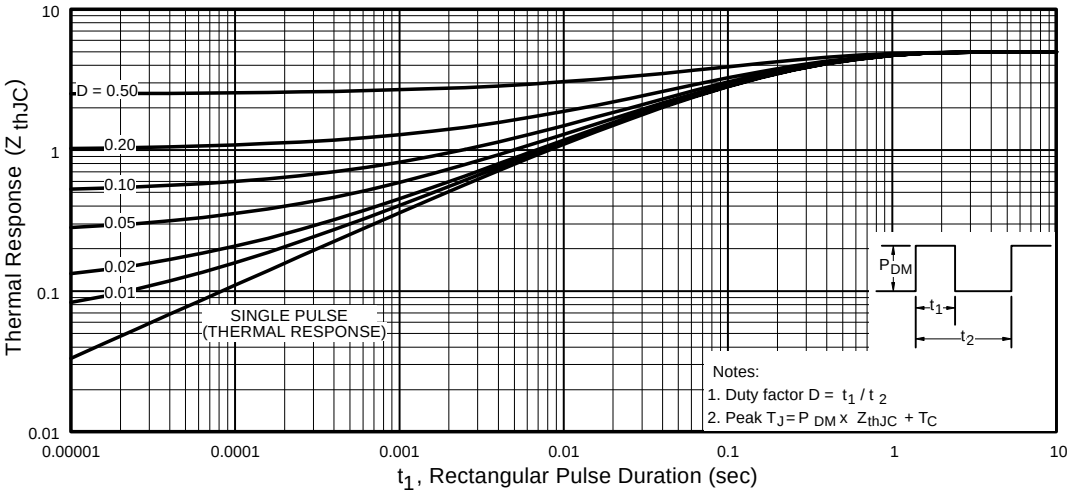


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

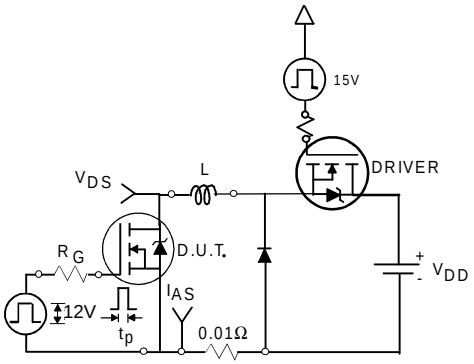


Fig 12a. Unclamped Inductive Test Circuit

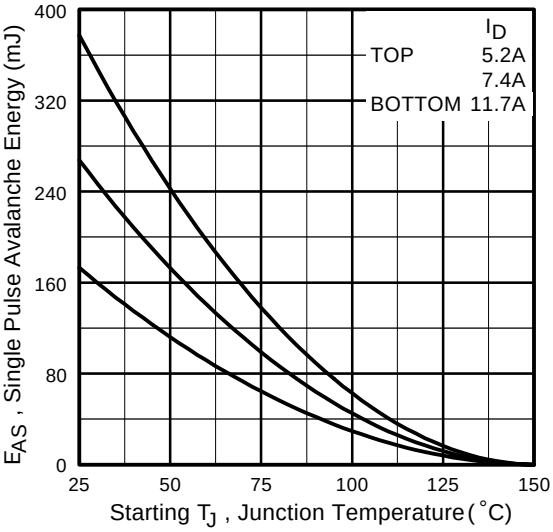


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

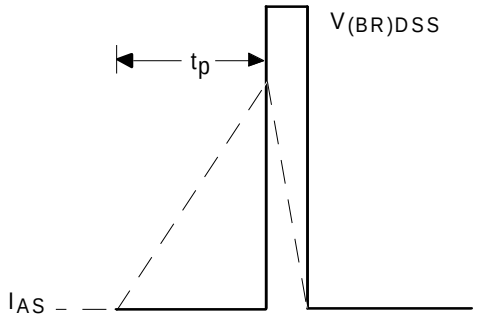


Fig 12b. Unclamped Inductive Waveforms

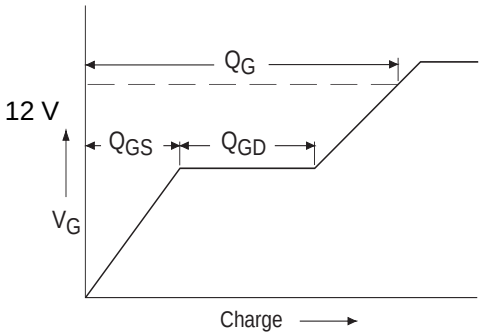


Fig 13a. Basic Gate Charge Waveform

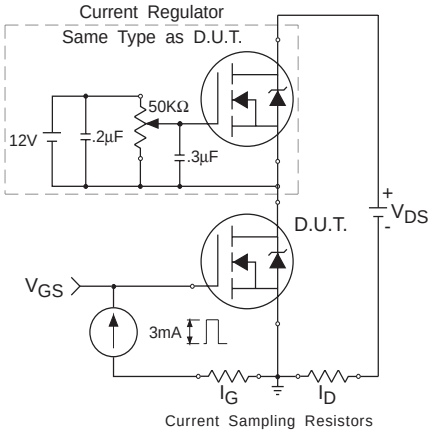


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L= 2.53 mH Peak I_L = 11.7A, V_{GS} = 12V

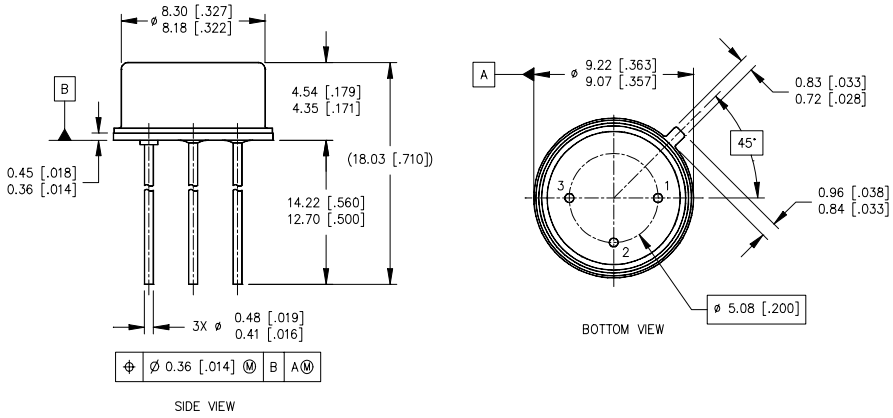
③ I_{SD} ≤ 11.7A, di/dt ≤ 216A/µs, V_{DD} ≤ 100V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — TO-205AF (Modified TO-39)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO–205AF (TO–39).

LEGEND
1- SOURCE
2- GATE
3- DRAIN

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 3/00